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Design and Characterization of a 5.2 GHz/2.4 GHz ΣΔ Fractional-N Frequency Synthesizer for Low-Phase Noise Performance

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This paper presents a complete noise analysis of a ΣΔ-based fractional-N phase-locked loop (PLL) based frequency synthesizer. Rigorous analytical and empirical formulas have been given to model various phase noise sources and spurious components and to predict their impact on the overall synthesizer noise performance. These formulas have been applied to an integrated multiband WLAN frequency synthesizer RFIC to demonstrate noise minimization through judicious choice of loop parameters. Finally, predicted and measured phase jitter showed good agreement. For an LO frequency of 4.3 GHz, predicted and measured phase noise was 0.50° rms and 0.535° rms, respectively.

1. INTRODUCTION

High-speed frequency synthesis is one of the most challenging areas in radio frequency integrated circuit (RFIC) design. It requires diverse knowledge of both high-speed analog and digital circuits as well as deep knowledge of system level issues. The performance requirements on circuits used for frequency synthesis are often extremely demanding making the design of these blocks even more challenging. However, a high-performance frequency synthesizer is a key component in many wired (fiber or cable) and wireless communication systems.

For modern multistandard applications, it is often difficult to cover multiple frequency bands using classical integer-N frequency synthesizers whose step size is limited by the reference frequency. In order to achieve fine step size to cover the multiband channel frequencies, one has to lower the reference frequency in an integer-N synthesizer design, which results in high division ratio of the PLL and thus high in-band phase noise. In contrast, a fractional-N synthesizer allows the PLL to operate with a high reference frequency while achieving fine step size by constantly swapping the loop division ratio between integer numbers, thus the average division ratio is a fractional number [1–4]. However, fine step size and low in-band phase noise is achieved with the penalty of fractional spurious tones, which come from the periodical division ratio variation. To remove the fractional spurious components for a synthesizer with fine step size, the best solution is to employ a ΣΔ noise shaper to control a programmable divider. A ΣΔ noise shaper will help to move large spurs to higher frequencies where they can be easily filtered. While spurs are often one of the most important design considerations for a frequency synthesizer, they will not be treated in detail in this paper. Since these techniques are becoming more and more common in modern synthesizer design, noise in this style of synthesizer will be the focus of this paper.

Here, a theoretical analysis of phase noise in modern frequency synthesizers will be presented. Phase noise is often the most challenging and crucial performance specification that must be met by a synthesizer. It is also the specification that often proves the most difficult to model and simulate. In this paper, a review of basic phase noise concepts will be presented, followed by a model that will allow the designer to take noise data from individual circuit simulations and predict the overall phase noise performance of an entire PLL frequency synthesizer.

The proposed analytical model will then be used to predict and optimize the phase noise performance of a ΣΔ fractional-N frequency synthesizer designed for multiband

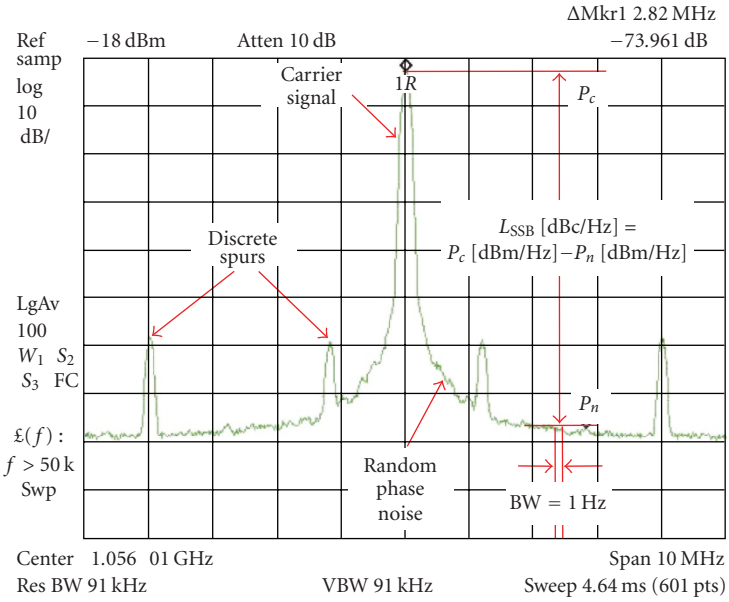

Figure 1: An example of phase noise and spurs at the synthesizer output observed using a spectrum analyzer.

WLAN applications. The comparison between the simulated and the measured phase noise demonstrates that the analytical model can accurately predict the performance of the complete synthesizer, and provide the designer with a quick and reliable means to predict the phase noise performance of a synthesizer RFIC prior to its fabrication.

2. BASIC PHASE NOISE CONCEPTS

Noise in synthesizers is contributed from all the building block circuits and components that make up the PLL. Synthesizer noise performance is usually expressed as phase noise, which is a measure of how much the output differs from an ideal impulse function in the frequency domain. We are primarily concerned with noise that causes fluctuations in the phase of the output rather than noise that causes fluctuations in the amplitude, since the output typically has a fixed and limited amplitude. The output of a synthesizer can be described as

$$v_{\text{out}}(t) = V_o \sin\left(\omega_{\text{LO}} t + \varphi_n(t)\right), \tag{1}$$

where $\omega_{\text{LO}} t$ is the desired phase of the output and $\varphi_n(t)$ is the time-variant random phase fluctuation of the output signal due to any noise sources in the PLL. Phase noise is often quoted in units of dBc/Hz or rad^2/Hz.

The phase fluctuation term $\varphi_n(t)$ in (1) may be random phase noise or discrete spurious tones, also called spurs, as shown in Figure 1. The discrete spurs at a synthesizer output are most likely due to the fractional-N mechanism, while the phase noise in an oscillator is mainly due to thermal, flicker, or $1/f$ noise and the finite Q of the oscillator tank. Assume the phase fluctuation is of a sinusoidal form as

$$\varphi(t) = \varphi_p \sin\left(\omega_m t\right), \tag{2}$$

where φ_p is the peak phase fluctuation and ω_m is the offset frequency from the carrier. Substituting (2) into (1) gives

$$\begin{aligned} v_{\text{out}}(t) &= V_0 \cos\left[\omega_c t + \varphi_p \sin\left(\omega_m t\right)\right] \\ &= V_0\left[\cos\left(\omega_c t\right)\cos\left(\varphi_p \sin\left(\omega_m t\right)\right)\right. \\ &\quad \left. - \sin\left(\omega_c t\right)\sin\left(\varphi_p \sin\left(\omega_m t\right)\right)\right]. \end{aligned} \tag{3}$$

For a small phase fluctuation, the above equation can be simplified as

$$\begin{aligned} v_0(t) &= V_0\left[\cos\left(\omega_c t\right) - \varphi_p \sin\left(\omega_m t\right)\sin\left(\omega_c t\right)\right] \\ &= V_0\left[\cos\left(\omega_c t\right) - \frac{\varphi_p}{2}\left[\cos\left(\omega_c + \omega_m\right)t - \cos\left(\omega_c - \omega_m\right)t\right]\right]. \end{aligned} \tag{4}$$

It is now evident that the phase-modulated signal includes the carrier signal tone and two symmetric sidebands at any offset frequency, as shown in Figure 1. A spectrum analyzer measures the phase noise power in dBm/Hz, but often phase noise is reported relative to the carrier power as

$$\text{PN}(\Delta\omega) = \frac{\text{Noise}\left(\omega_{\text{LO}} + \Delta\omega\right)}{P_{\text{carrier}}\left(\omega_{\text{LO}}\right)}, \tag{5}$$

where *Noise* is the noise power in a 1 Hz bandwidth and P_{carrier} is the power of the carrier or local oscillator (LO) tone at the frequency at which the synthesizer is operating. In this form, phase noise has the units of [rad^2/Hz]. Often this is quoted as so many dB down from the carrier in units of [dBc/Hz]. To further complicate this, both single-sideband and double-sideband phase noise can be defined. Single-sideband (SSB) phase noise is defined as the ratio of power in one phase modulation sideband per Hertz bandwidth, at an offset $\Delta\omega$ away from the carrier, to the total signal power. The SSB phase noise power spectral density (PSD)

to carrier ratio, in units of [dBc/Hz], is defined as

$$\mathrm{PN}_{\mathrm{SSB}}(\Delta\omega) = 10\log\left[\frac{N(\omega_{\mathrm{LO}}+\Delta\omega)}{P_{\mathrm{carrier}}(\omega_{\mathrm{LO}})}\right]. \tag{6}$$

Combining (4) into (6) this equation can be rewritten as

$$\begin{aligned}\mathrm{PN}_{\mathrm{SSB}}(\Delta\omega) &= 10\log\left[\frac{(1/2)(V_0\varphi_p/2)^2}{(1/2)V_0^2}\right]\\ &= 10\log\left[\frac{\varphi_p^2}{4}\right] = 10\log\left[\frac{\varphi_{\mathrm{rms}}^2}{2}\right],\end{aligned} \tag{7}$$

where φ_{rms}^2 is the rms phase noise power density in units of [rad^2/Hz]. Note that single-sideband phase noise is by far the most common type reported and often it is not specified as SSB, but rather simply reported as phase noise. However, alternatively double-sideband phase noise can be expressed by

$$\begin{aligned}\mathrm{PN}_{\mathrm{DSB}}(\Delta\omega) &= 10\log\left[\frac{N(\omega_{\mathrm{LO}}+\Delta\omega)+N(\omega_{\mathrm{LO}}-\Delta\omega)}{P_{\mathrm{carrier}}(\omega_{\mathrm{LO}})}\right]\\ &= 10\log\left[\varphi_{\mathrm{rms}}^2\right].\end{aligned} \tag{8}$$

From either the single-sideband or double-sideband phase noise, the rms phase noise can be obtained in the linear domain as

$$\begin{aligned}\varphi_{\mathrm{rms}}(\Delta\omega) &= \frac{180}{\pi}\sqrt{10^{\mathrm{PN}_{\mathrm{DSB}}(\Delta\omega)/10}}\\ &= \frac{180\sqrt{2}}{\pi}\sqrt{10^{\mathrm{PN}_{\mathrm{SSB}}(\Delta\omega)/10}}[\mathrm{deg}/\sqrt{\mathrm{Hz}}].\end{aligned} \tag{9}$$

It is also quite common to quote integrated phase noise over a certain bandwidth. The rms-integrated phase noise of a synthesizer is given by

$$\mathrm{IntPN}_{\mathrm{rms}} = \sqrt{\int_{\Delta\omega_1}^{\Delta\omega_2}\varphi_{\mathrm{rms}}^2(\omega)d\omega}. \tag{10}$$

The limits of integration are usually the offsets corresponding to the lower and upper frequencies of the bandwidth of the information being transmitted.

In addition, it should be noted that dividing or multiplying a signal in the time domain also divides or multiplies the phase noise. Similarly, if a signal is translated in frequency by a factor of N, then the phase noise power is increased by a factor of N^2 as

$$\begin{aligned}\varphi_{\mathrm{rms}}^2(N\omega_{\mathrm{LO}}+\Delta\omega) &= N^2\cdot\varphi_{\mathrm{rms}}^2(\omega_{\mathrm{LO}}+\Delta\omega),\\ \varphi_{\mathrm{rms}}^2\left(\frac{\omega_{\mathrm{LO}}}{N}+\Delta\omega\right) &= \frac{\varphi_{\mathrm{rms}}^2(\omega_{\mathrm{LO}}+\Delta\omega)}{N^2}.\end{aligned} \tag{11}$$

Note this assumes that the circuit that did the frequency translation is noiseless. Otherwise, additional phase noise will be added. Also, note that the phase noise is scaled by N^2 rather than N because we are dealing with noise in units of power rather than units of voltage.

3. BUILDING BLOCK PHASE NOISE MODELS FOR PLL SYNTHESIZER

Next, we will present the phase noise models for all PLL synthesizer building blocks such as the crystal oscillator, divider, phase-frequency detector (PFD), charge pump (CP), loop lowpass filter (LPF), and voltage-controlled oscillator (VCO). While the circuit-or block-level simulation of a typical synthesizer design will not be discussed in detail in this paper, some basic theory will be presented to show how the noise in each block can affect the loop performance. In Section 4, the effect of these noise sources on a complete synthesizer will be examined.

3.1. VCO noise

The phase noise from a VCO can be described as [5, 6]

$$\varphi_{\mathrm{VCO}}^2(\Delta\omega) = \left(\frac{\omega_o}{(2Q\Delta\omega)}\right)^2\left(\frac{GkT}{2P_S}\right)\left(1+\frac{\omega_c}{\Delta\omega}\right), \tag{12}$$

where P_S is the signal power of the carrier, T is the temperature, Q is the quality factor of the oscillator's resonator, k is Boltzmann's constant, ω_o is the frequency of oscillation, ω_c is the flicker noise corner frequency, and G is a constant of proportionality which takes into account excess noise from the VCO transistors, and nonlinearity. Note that many additional refinements have been made to this formula, however as given here it is sufficient to capture the shape of most integrated VCO's phase noise. Thus, at most frequencies of interest, the phase noise produced by the VCO will decrease at 20 dB/decade for an increasing offset frequency away from the carrier. This will not continue indefinitely, as thermal noise will put a lower limit on this phase noise which for most integrated VCOs is somewhere between -120 and -150 dBc/Hz. VCO phase noise is usually dominant outside the loop bandwidth and of less importance at low offset frequencies.

3.2. Crystal reference noise

Crystal resonators are widely used in frequency control applications because of their unequaled combination of high Q, stability, and small size. The resonators are classified according to "cut," which is the orientation of the crystal wafer (usually made from quartz) with respect to the crystallographic axes of the material. The total noise power spectral density of a crystal oscillator can also be found from Leeson's formula and making use of a typical empirical multiplier [7]:

$$\varphi_{\mathrm{XTAL}}^2(\Delta\omega) = 10^{-16\pm1}\cdot\left[1+\left(\frac{\omega_0}{2\Delta\omega\cdot Q_L}\right)^2\right]\left[1+\frac{\omega_c}{\Delta\omega}\right], \tag{13}$$

where ω_0 is the oscillator output frequency, ω_c is the corner frequency between $1/f$ and thermal noise regions, which is normally in the range 1–10 kHz, Q_L is the loaded quality factor of the resonator. Since Q_L for crystal resonator is very large (normally in the order of 10^4 to 10^6), the reference noise

contributes only to the very close-in noise and it quickly reaches thermal noise floor at offset frequency around ω_c.

3.3. Frequency divider noise

Frequency dividers consist of switching logic circuits, which are sensitive to the clock timing jitter. The jitter in the time domain can be converted to phase noise in the frequency domain. Time jitter or phase noise occurs when rising and falling edges of digital dividers are superimposed with spurious signals such as Johnson and flicker noise in semiconductor materials. Ambient effects result in variation of the triggering level due to temperature and humidity. Frequency dividers generate spurious noise especially for high-frequency operation. Dividers do not generate signals, but rather simply change their frequency. Kroupa provided an empirical formula, which estimates the amount of phase noise that frequency dividers add to a signal [8, 9]:

$$\varphi^2_{\text{Div\_Added}}(\Delta\omega) \approx \frac{10^{-14\pm1} + 10^{-27\pm1}\omega^2_{\text{do}}}{2\pi\cdot\Delta\omega} + 10^{-16\pm1} + \frac{10^{-22\pm1}\omega_{\text{do}}}{2\pi}, \tag{14}$$

where ω_{do} is the divider output frequency and $\Delta\omega$ is the offset frequency. Notice that the first term in (14) represents the flicker noise and the second term gives the white thermal noise floor. The third term is caused by timing jitter due to coupling, ambient, and supply variations.

3.4. Phase detector noise

Phase detectors experience both flicker and thermal noise. At large offsets, phase detectors generate a white phase noise floor typically about -160 dBc/Hz, which is thermal noise-dominant. The noise power spectral density of phase detectors is estimated empirically by [9]

$$\varphi^2_{\text{PD}}(\Delta\omega) \approx \frac{2\pi\cdot10^{-14\pm1}}{\Delta\omega} + 10^{-16\pm1}. \tag{15}$$

3.5. Charge pump noise

The noise of the charge pump can be characterized as an output noise current and is usually given in pA/$\sqrt{\text{Hz}}$. Note that at this point in the loop, current represents the phase. The charge pump output current noise can be a strong function of the reference frequency and width of the current pulses. Therefore, for low-noise operation it is desirable to keep the charge pump sink and source currents matched as well as possible. This is because current sources only produce noise when they are on. When an ideal loop is locked, the sink and source current sources in a charge pump are turned off, resulting in zero net current charge or discharge of the holding capacitor. However, nonidealities result in finite pulses that will turn on the source and sink currents for about the same amount of time. The closer reality matches the ideal case, the less noise will be produced. Also, note that as the offset frequency is decreased, $1/f$ noise will become more important, causing the noise to increase. This noise can often be the dominant noise source at low-frequency offsets. Charge pump noise can be simulated with proper tools such as Cadence pss pnoise analysis. The results depend on the design in question so no simple general analytical formula will be given here, however, an example will be given later.

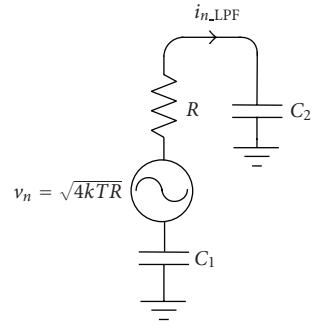

Figure 2: Loop filter with thermal noise added.

3.6. Loop filter noise

Loop filters can be analyzed for noise in the frequency domain in a linear manner. The most common loop filter that will be examined in this paper will now be analyzed. It consists of two capacitors and one resistor. For offchip filters, the loss experienced by capacitors is negligible. Thus, the loop filter contains only one noise source, the thermal noise associated with the resistor R. The loop filter with its associated noise source can be drawn as shown in Figure 2. Now the noise voltage develops a current flowing through the series combination of C_1, C_2, and R (assuming that the CP and VCO are both open circuits), which is given by

$$i_{n\_\text{LPF}} = \frac{1}{R}\cdot\frac{v_n s}{s + (C_1 + C_2)/C_1C_2R} \approx \frac{1}{R}\cdot\frac{v_n s}{s + 1/C_2R}. \tag{16}$$

Thus, this noise current will have a highpass characteristic, and therefore the loop will not produce any noise at DC and this noise will increase until the highpass corner is reached, after which it will be flat. Other filters can be analyzed in a similar manner.

3.7. Phase noise due to ΣΔ converters

Fractional-N synthesizers often include ΣΔ modulators to shift the spurious components to a higher-frequency band, where the loop filter can filter randomized spurs. In a ΣΔ fractional-N synthesizer, the average loop divisor value corresponds to the desired output frequency and the instantaneous divisor value is dithered around the correct value by

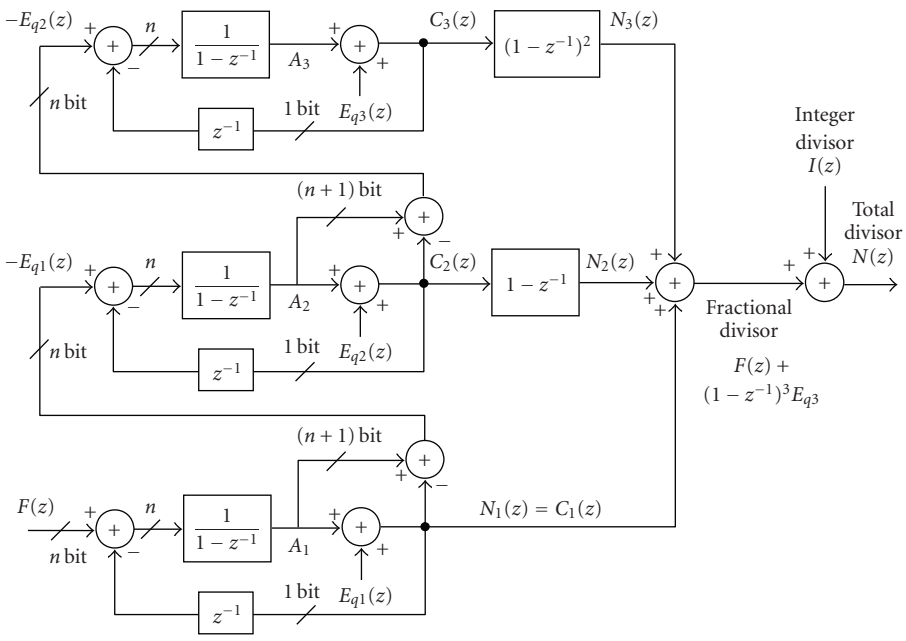

Figure 3: A three-loop MASH 1-1-1 ΣΔ modulator for fractional-N synthesis.

the ΣΔ modulator. The ΣΔ noise shaping can be modeled as a linear gain stage with an additive quantization noise source, which is shaped by a highpass transfer function. Hence, the quantization error component at the synthesizer output is composed of mostly high-frequency noise that can be filtered by the PLL. A block diagram of a typical ΣΔ modulator that is widely used in synthesizer applications is shown in Figure 3 [3]. This three-loop sigma-delta topology is called a MASH 1-1-1 structure, because it is a cascaded ΣΔ structure with three first-order loops. Each of the three loops is identical. The input of the second loop is taken from the quantized error E_{q1} of the first loop, while the input of the third loop is taken from the quantized error E_{q2} of the second loop. Thus, only the first loop has a constant input, which is the fractional portion of the desired rational divide number $F(z)$, that is, the fine tune word. The integer part of the frequency word $I(z)$, the coarse tune word, is added at the output of the three-loop ΣΔ modulator. Thus, $N_{\text{div}}(z) = I(z) + F(z)$ is the time sequence used to control the integer-restricted divider ratios. The modulator is clocked at the divider output frequency, reflecting the sampled nature of the circuit.

The first loop generates the fractional divisor value $F(z)$ with the byproduct of quantization error E_{q1}, which is further fed to the input of the second loop for further processing. The second loop cancels the previous loop's quantization error E_{q1} by the additional filter block $(1 - z^{-1})$ in its output path. The only quantization noise term left after summing the first and second loop outputs is the quantization error E_{q2}, which is second-order noise-shaped. When this noise term is further fed to the input of the third loop, the loop generates a negative noise term to cancel the previous loop's quantization error E_{q2} by the additional filter block $(1-z^{-1})^2$ in its output path. Summing the outputs of the three loops, we obtain the modulated divisor value as

$$\begin{aligned} N(z) &= I(z) + N_1(z) + N_2(z) + N_3(z) \\ &= I(z) + F(z) + \left(1 - z^{-1}\right)^3 E_{q3}(z), \end{aligned} \tag{17}$$

where $I(z)$ and $F(z)$ are the integer portion and the fractional portion of the division ratio, respectively. As desired, the fractional divisor value $F(z)$ is not affected by the modulator, while the quantization error generated in the last loop E_{q3} is noise-shaped by a third-order highpass function of $(1 - z^{-1})^3$. The quantization error generated in the first and second loops are totally canceled, and as a result the total quantization noise is equal to that of a single loop, although three loops are used. Therefore, the multiloop sigma-delta architecture provides high-order noise shaping without additional quantization noise.

Discrete fractional spurs are generated by this circuit at multiples of the reference frequency, but these spurs become more like random noise after sigma-delta noise shaping. The single-sideband phase noise of the noise-shaped fractional spurs can be analyzed as follows. The 1-bit quantization error power is $\Delta^2/12$ where Δ is the quantization step size. For $\Delta = 1$, which is the case for a truncated binary word, the quantization error power is 1/12. This error power is spread over the sampling bandwidth, or equivalently the reference bandwidth of $f_r = 1/T_s$. Thus, the error power spectral density (PSD) becomes $1/(12f_r)$. Considering the noise shaping with an mth-order MASH ΣΔ modulator as expressed in (17), the frequency noise PSD is obtained as

$$S_\Omega(z) = \frac{\left|\left(1 - z^{-1}\right)^m f_r\right|^2}{12 f_r} = \frac{1}{12}\left(1 - z^{-1}\right)^{2m} f_r, \tag{18}$$

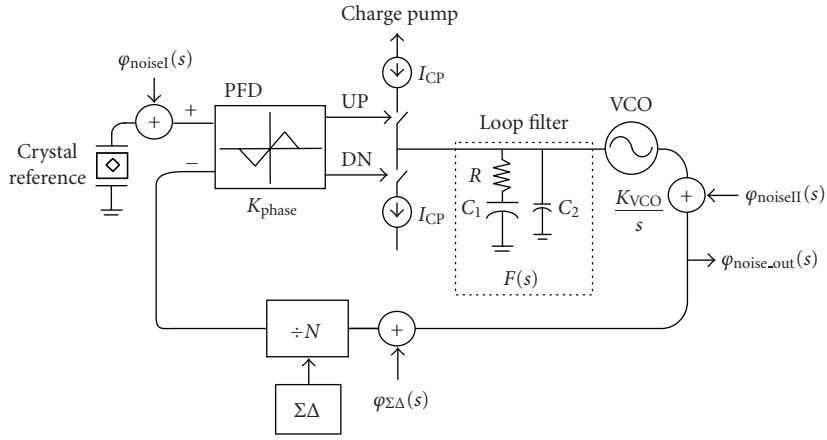

Figure 4: A synthesizer showing places where noise is injected.

where the subscript Ω denotes the frequency fluctuations referred to the *input* of the divider. In order to obtain the phase fluctuations, consider the following relationship between frequency and phase:

$$\omega(t) = \frac{d\phi(t)}{dt} \approx \frac{\phi(t) - \phi(t - T_s)}{T_s} \tag{19}$$

and its z-domain representation of

$$2\pi \cdot \Omega(z) = \frac{\Phi(z)(1 - z^{-1})}{T_S}, \tag{20}$$

where $T_s = 1/f_r$ is the sample period and where multiplication by z^{-1} represents a delay of T_s. Rearranging this expression yields

$$\Phi(z) = \frac{2\pi \cdot \Omega(z)}{f_r(1 - z^{-1})}. \tag{21}$$

Noting that $S_\Omega(z)$ is given in terms of power, the double-sideband phase noise PSD is obtained as

$$\begin{aligned} S_\Phi(z) &= S_\Omega(z)\frac{(2\pi)^2}{|1 - z^{-1}|^2 f_r^2} \\ &= \frac{(2\pi)^2}{|1 - z^{-1}|^2 f_r^2} \cdot \frac{1}{12}(1 - z^{-1})^{2m} f_r \\ &= \frac{(2\pi)^2}{12 f_r} \cdot (1 - z^{-1})^{2m-2}, \end{aligned} \tag{22}$$

where the subscript Φ denotes phase fluctuations. Noting that

$$(1 - z^{-1}) = |1 - e^{-j\omega T}| = 2\sin\left(\frac{\omega T}{2}\right) = 2\sin\left(\frac{\pi f}{f_r}\right), \tag{23}$$

the single-sideband phase noise PSD in the frequency domain is given by

$$\begin{aligned} \frac{\varphi^2_{\Sigma\Delta}(f)[\text{rad}^2/\text{Hz}]}{2} &= \frac{(2\pi)^2}{24 f_r} \cdot \left[2\sin\left(\frac{\pi f}{f_r}\right)\right]^{2(m-1)}, \\ \text{PN}(f)[\text{dBc/Hz}] &= 10\log\left\{\frac{(2\pi)^2}{24 f_r} \cdot \left[2\sin\left(\frac{\pi f}{f_r}\right)\right]^{2(m-1)}\right\}. \end{aligned} \tag{24}$$

4. IN-BAND AND OUT-OF-BAND PHASE NOISE IN PLL SYNTHESIS

A typical PLL-based synthesizer system level diagram that will be analyzed in this paper is shown in Figure 4. It consists of a phase-frequency detector, a charge pump, a loop filter, a VCO, a programmable divider, a reference oscillator (typically a crystal reference source), and a fractional accumulator with $\Sigma\Delta$ modulation circuit to achieve the fine synthesizer step size without impacting the phase noise performance.

The noise transfer functions for the various noise sources in the loop can be derived using conventional control theory [9, 10]. There are three additive noise transfer functions: one for the VCO noise, that is, the contributor of the synthesizer out-of-band noise, one for the $\Sigma\Delta$ modulator noise that could contribute to both in-band and out-of-band noise, and one for all other noise sources such as the PFD, CP, divider, and loop filter that are the contributors of the in-band noise. All in-band noise sources are referred back to the input of the PLL and shown as φ_{noiseI} in Figure 4. The noise from the VCO is referred to the output and represented by φ_{noiseII} in Figure 4, while the noise from the $\Sigma\Delta$ modulator is shown as $\varphi_{\Sigma\Delta}$. The noise transfer function (NTF) for in-band noise $\varphi_{\text{noiseI}}(s)$ is given by

$$\frac{\varphi_{\text{noise\_out}}(s)}{\varphi_{\text{noiseI}}(s)} = \frac{(IK_{\text{VCO}}/2\pi \cdot C_1)(1 + RC_1 s)}{s^2 + (IK_{\text{VCO}}/2\pi \cdot N)Rs + IK_{\text{VCO}}/2\pi \cdot NC_1}. \tag{25}$$

As shown, the in-band noise transfer function has a lowpass characteristic. Note that for low-frequencies inside the loop bandwidth, the loop will track the input phase including the input phase noise. Therefore, this noise will be transferred to the PLL output. At higher offset frequencies, this noise is suppressed by the loop's lowpass filter. Thus, the noise coming from the PFD, CP, divider, and loop filter contributes to the in-band noise at the PLL output. Also, note that the division ratio plays a very important role in this transfer function. Within the loop bandwidth, the in-band phase noise is magnified N times by the loop. Therefore, choosing smaller divisor value N will benefit the in-band noise reduction.

The VCO noise transfer function is slightly different. In this case, setting the input reference and input noise source to zero, the VCO noise transfer function is given by

$$\frac{\varphi_{\text{noise\_out}}(s)}{\varphi_{\text{noiseII}}}(s) = \frac{s^2}{s^2 + (IK_{\text{VCO}}/2\pi \cdot N)Rs + IK_{\text{VCO}}/2\pi \cdot NC_1}. \tag{26}$$

As shown, the VCO noise transfer function has a highpass characteristic. Thus, at low offsets inside the loop bandwidth the VCO noise is suppressed by the feedback loop, yet outside the loop bandwidth the VCO is essentially free running without noise attenuation. Thus, the out-of-band PLL noise approaches the VCO noise.

The noise transfer function of the ΣΔ modulator is very similar to the in-band noise transfer function except an extra $1/N$ term in the numerator as the ΣΔ is not input-referred. Note that due to the highpass nature of the ΣΔ NTF, the order of the loop roll-off is very important. The noise shaping slope of an mth-order MASH ΣΔ modulation is $20(m-1)$ dB/decade according to (24), while an nth-order lowpass loop filter has a roll-off slope of $20n$ dB/decade. Therefore, the order of loop filter must be higher than or equal to the order of the ΣΔ modulator in order to attenuate the out-of-band noise due to ΣΔ modulation. Thus, for instance, when calculating the effect of the ΣΔ modulator on out-of-band noise on the typical loop, it is necessary to include additional capacitor C_2 in the loop filter as this will provide extra attenuation out of band. In this case, the ΣΔ noise transfer function to the output would be

$$\frac{\varphi_{\text{noise\_out}}(s)}{\varphi_{\Sigma\Delta}(s)} = \frac{K_{\text{VCO}}K_{\text{phase}}(1+sC_1R)}{s^2N(C_1+C_2)(1+sC_sR) + K_{\text{VCO}}K_{\text{phase}}(1+sC_1R)}, \tag{27}$$

where $C_s = C_1C_2/(C_1+C_2)$.

5. CIRCUIT-LEVEL PHASE NOISE COMPONENTS

The methods for dealing with phase noise will now be considered with application to an actual synthesizer RFIC design case. The results of the analysis can then be verified against measurement data. The synthesizer to be considered was designed using a 47 GHz 0.5 μm BiCMOS process using primarily the CMOS part of the technology. The only exceptions were some high-speed bipolar CML in the divider and the output buffer circuits. The rest of the synthesizer including the VCO cores was all CMOS. It was designed for multiband WLAN applications, and had a reference frequency of 40 MHz, a fairly standard charge pump and PFD configuration with gain K_{phase} of 750 μA/2π, a multimodulus divider programmable between 64 and 127, and an LC-based VCO with a K_{VCO} of approximately 120 MHz/V. The synthesizer was designed to generate carrier frequencies in the range from 3.2 to 3.3 GHz and from 4.1 to 4.3 GHz. The MMD gives a total division ratio of 86–88 and 102–108 under normal operating conditions and was controlled by a third-order ΣΔ modulator to provide the needed step size and noise shaping. The crystal oscillator used as a reference for this design had a Q_L of 8×10^4 and a noise floor of −150 dBc/Hz. The details of the actual circuit implementation will not be discussed in this paper, but are similar to those given in [11]. The raw VCO phase noise can be either predicted from a calculation [6] or else simulated with the aid of spectre or some other simulator. Output current noise from the charge pump/PFD combination can also be simulated or predicted from transistor level noise calculations. This simulation must be done using driving signals in the locked state to simulate accurately the amount of time the CP spends in the on state. This simulation can be used to predict how much noise current is on average produced by the circuit. Likewise simulations on the divider can be performed. The crystal oscillator is normally a commercially available part and data on its phase noise performance is often available from the manufacturer. The ΣΔ phase noise can be estimated from (24). Note that the maximum fractionality used in this design was 1/32. While this had an impact on the spurs of the system in different channels, the third-order ΣΔ has kept all the spurs below −50 dBc level such that the fractional spurs did not affect the phase noise of the system. Such simulations and calculations were performed for the sample design. The results of all raw phase noise due to circuit components are plotted in Figure 5. All phase noise is referred to the VCO output frequency for easy comparison of the relative importance of the phase noise sources.

Next the optimal loop bandwidth for best phase noise performance must be determined. To do this the following must be implemented.

(1) Plot all phase noise components.
(2) Determine the intercept point of ΣΔ and VCO noise.
(3) Compare it to the intercept between VCO noise and in-band noise (normally dominated by charge pump noise).
(4) If the ΣΔ intercepts the VCO noise at a lower frequency than the in-band noise does, a higher-order ΣΔ is needed to prevent in-band noise degradation. Then make sure the higher-order ΣΔ noise intercepts the VCO noise at a higher frequency than the in-band noise does.

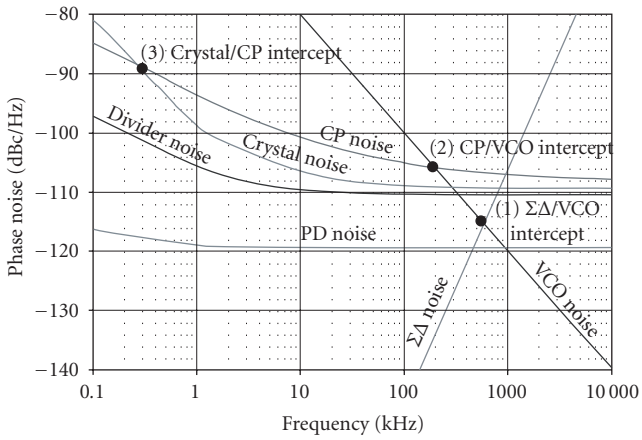

Figure 5: A plot of all raw phase noise components for the design referred to the VCO output frequency.

(5) Choose the intercept between the out-of-band noise (VCO noise) and the in-band noise (CP noise, reference noise, divider noise, etc.) as the loop optimal bandwidth.

As an example, consider the plot of Figure 5. First the ΣΔ modulator used in the design must be considered. Since this noise increases with offset frequency, the loop bandwidth must be set low enough to properly attenuate this noise and prevent it from growing to dominate the phase noise of the design. Thus the loop bandwidth must be set lower than the intercept of the VCO noise and the ΣΔ noise (see point No.1 in Figure 5 at 600 kHz offset). For this design at frequencies between 300 Hz and 200 kHz, the in-band noise is dominated by CP, which is a fairly typical occurrence. This noise must also be weighed against the VCO noise and the intercept of these two noise sources (see point No.2 in Figure 5 at 200 kHz offset). Note that this point is lower than the ΣΔ intercept with the VCO noise and therefore it is the crucial point in this case that sets the loop bandwidth. Thus the loop bandwidth should be set at the point where these two noise sources are equal. Setting the loop bandwidth wider would result in the loop phase noise being dominated by the CP when it could be dominated by the lower VCO noise, and setting the loop bandwidth lower than this will result in the loop phase noise being dominated by the VCO, when it could be dominated by the lower CP/PFD noise. Thus, in this design the optimum loop bandwidth can be determined from the plot as the cross-over point between these two curves at an offset frequency of 200 kHz. Therefore the best possible out-of-band phase noise is the raw phase noise of the VCO and the in-band phase noise will be dominated by the CP above a frequency of 300 Hz. Below this frequency the crystal oscillator noise will dominate the in-band noise (see point No.3 in Figure 5 at 300 Hz offset).

6. COMPLETE PHASE NOISE ANALYSIS AND COMPARISON WITH MEASUREMENTS

Having determined the optimum loop bandwidth for best phase noise performance, the overall loop phase noise performance can be predicted with the aid of the theory developed in Section 4. The loop filter components were chosen as shown in Table 1. A ratio of only 5 : 1 was chosen for C_1 and C_2 to help attenuate high-frequency ΣΔ phase noise and also to provide additional spur rejection. This can cause slight additional peaking in the phase noise at the loop corner frequency, but had a negligible impact on the integrated phase noise. Note that additional poles in the loop filter could lead to improved out-of-band performance, but since the loop filter was external in this experiment, this would have required additional package pins.

Table 1: Loop filter components.

Parameter	Value
C_1	3 nF
C_2	600 pF
R	600 Ω

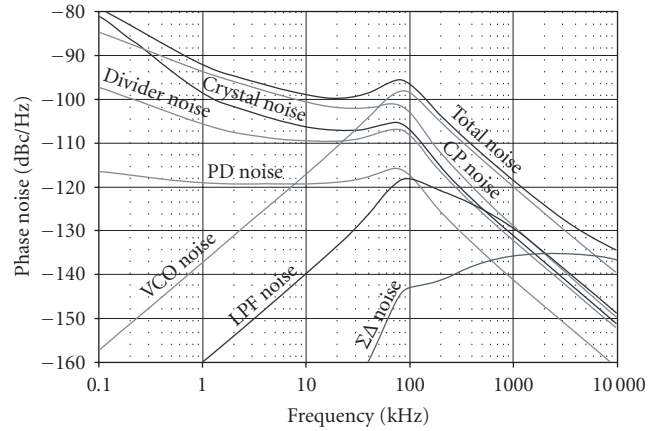

Figure 6: A plot of all phase noise including the effect of the loop.

The overall phase noise as well as all noise components are plotted in Figure 6 for a divider ratio of 87. The phase noise for this design integrated from 100 Hz to 10 MHz was predicted to be 0.44° rms.

The synthesizer was fabricated and embedded with the rest of the circuitry that formed the WLAN transceiver. The back end of the process featured thick aluminum metallization designed to provide high-quality inductors. A die photo of the synthesizer is shown in Figure 7. This particular design implemented three VCO cores, however only two were required to cover all required WLAN frequencies. Each VCO had a tuning range of approximately 600 MHz. The synthesizer occupies an area of 2.3 mm by 1.4 mm. The synthesizer drew a current of 36 mA from a 2.75 V supply.

The measured and simulated phase noise is compared in Figure 8 for a division ratio of 87 and in Figure 9 for a division ratio of 105. The comparison demonstrates that the overall PLL noise performance is predicted very closely by simulation and calculation. Thus, the proposed analytic model provides a rigorous model for analyzing PLL

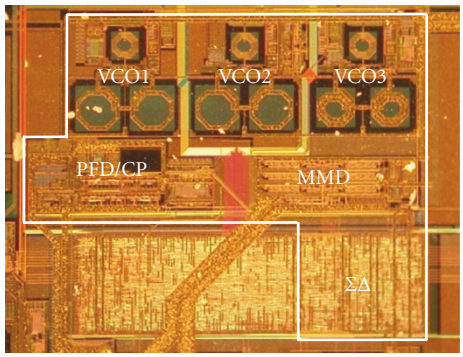

Figure 7: Die photograph of the synthesizer.

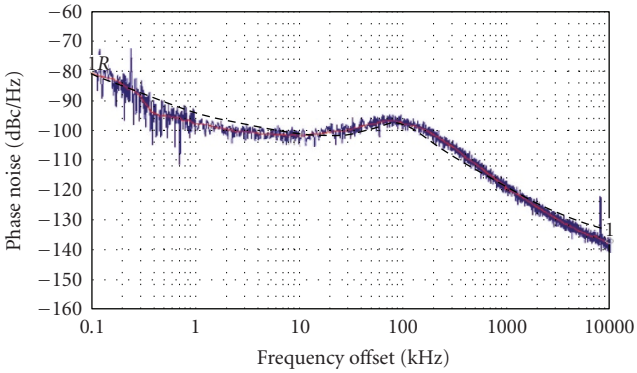

Figure 8: Comparison of measured and simulated phase noise for the 3.2-3.3 GHz band. The square dots are the simulated data.

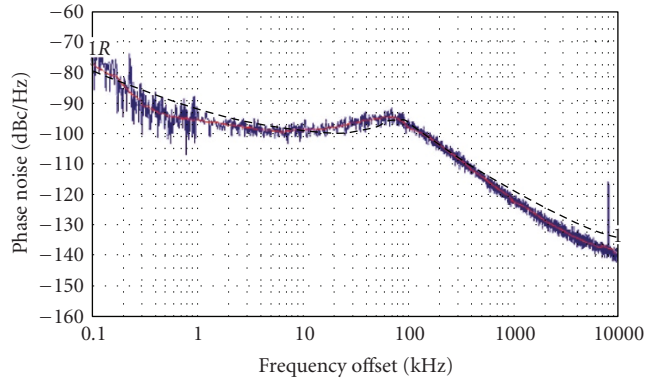

Figure 9: Comparison of measured and simulated phase noise for the 4.1–4.3 GHz band. The square dots are the simulated data.

Table 2: Comparison of measured and simulated phase noise.

Frequency band	Simulated phase noise	Measured phase noise
3.2-3.3 GHz	0.44° rms	0.50° rms
4.1-4.3 GHz	0.50° rms	0.535° rms

Table 3: Summary of synthesizer performance.

Parameter	Performance
Technology	0.5μ m BiCMOS
VCO phase noise	−120 dBc/Hz @ 1 MHz
In-band phase noise	−100 dBc/Hz @ 10 kHz
Loop corner frequency	200 kHz
Reference frequency	40 MHz
Number of accumulator/MMD bits	6
Order of ΔΣ accumulator	3rd
Synthesizer step size	468.75 kHz
Spurious	< −50 dBc
Power supply	2.75 V
Current consumption	36 mA
Synthesizer die area	3.22 mm^2

synthesizer phase noise performance. The model can serve as a design guide for synthesizer designers to optimize their circuits and meet their design goals prior to the expensive fabrication. The measured integrated phase noise of the WLAN synthesizer was 0.5° rms for the lower band and 0.535° rms for the upper band and that is close to the predicted phase noise. These results are summarized in Table 2.

Owing to the accuracy of the proposed phase noise model, we were able to optimize the synthesizer circuits for improved noise performance prior to fabrication. The overall measured and simulated phase noise performance of the synthesizer RFIC is summarized in Table 3. Note that in this work the synthesizer was integrated with a superheterodyne front-end with an IF of approximately 1 GHz, and thus the LO frequencies are offset from the WLAN frequency bands. Translating the frequency of the LO up or down will improve or degrade the phase noise by the ratio the center frequency is scaled. The achieved phase noise is also compared to the most recently published WLAN synthesizer designs in Table 4. As shown, this design achieved one of the best phase noise performances for integrated WLAN transceiver RFICs. Note that in this table the phase noise quoted was for the transceiver system and not simply of the synthesizers themselves.

7. CONCLUSIONS

In this paper, a rigorous analytical model for determining the phase noise performance of PLL-based fractional-N ΣΔ synthesizers has been presented. Noise due to voltage-controlled oscillators, charge pumps, crystal oscillators, phase-frequency detectors, charge pumps, loop filters, and ΣΔ modulator has been analyzed. Analyzing an example synthesizer RFIC designed for multiband MIMO WLAN applications has validated the theory. The analytical model achieved good agreements with measured synthesizer phase noise performance. The predicted phase noise of 0.44° rms and 0.50° rms at 3 GHz and 4 GHz bands, respectively,

Table 4: Comparison of synthesizer performance.

References	Frequency band (GHz)	Technology	Phase noise dBc/Hz @1 MHz	Phase noise dBc/Hz @10 kHz	Integrated phase noise of the system
[12]	2.4, 5.1–5.8	0.25 μm CMOS	−115	−105	0.7° rms, 5.3 GHz 1 kHz–10 MHz
[13]	5.1–5.8	0.18 μm CMOS	−115	−92	0.8° rms 1 kHz–10 MHz
[14]	5.1–5.3	0.18 μm CMOS	−110	−92	1.5 ∼ 2° rms 10 kHz–10 MHz
This work	2.4, 5.1–5.3	0.5 μm BiCMOS	−120	−98	0.4° rms, 2.4 GHz 0.7° rms, 5.3 GHz 100 Hz–10 MHz

agreed closely with the measured results of 0.5° rms and 0.535° rms.

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