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Novel Radio Architectures for UWB, 60 GHz, and Cognitive Wireless Systems

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There are several new radio systems which exploit novel strategies being made possible by the regulatory agencies to increase the availability of spectrum for wireless applications. Three of these that will be discussed are ultra-wideband (UWB), 60 GHz, and cognitive radios. The UWB approach attempts to share the spectrum with higher-priority users by transmitting at power levels that are so low that they do not cause interference. On the other hand, cognitive radios attempt to share spectra by introducing a spectrum sensing function, so that they are able to transmit in unused portions at a given time, place, and frequency. Another approach is to exploit the advances in CMOS technology to operate in frequency bands in the millimeter-wave region. 60 GHz operation is particularly attractive because of the 7 GHz of unlicensed spectrum that has been made available there. In this paper, we present an overview of novel radio architecture design approaches and address challenges dealing with high-frequencies, wide-bandwidths, and large dynamic-range signals encountered in these future wireless systems.

1. INTRODUCTION

The demand for wireless connectivity and crowding of unlicensed spectra has pushed the regulatory agencies to be ever more aggressive in providing new ways to use spectra. In the past, the approach for spectrum allocation was based on specific band assignments designated for a particular service, as illustrated by the Federal Communications Commission's (FCC) frequency allocation chart. This spectrum chart contains overlapping allocations in most frequency bands and seems to indicate a high degree of spectrum scarcity.

While spectrum efficiency of some radio systems is improving (e.g., cell phone and WiFi bands), they are faced with increasing interference that limits network capacity and scalability. On the other hand, some bands are poorly utilized. Measurements taken in downtown Berkeley (Figure 1) reveal a typical utilization of roughly 30% below 3 GHz, and 0.5% in the 3–6 GHz frequency band.

In order to promote more flexibility in spectrum sharing, the FCC has provided new opportunities for unlicensed spectrum usage with fewer restrictions on radio parameters. Three new opportunities in spectrum access have thus been introduced: (1) an underlay approach with severe restrictions on transmitted power levels with a requirement to operate over "ultra-" wide bandwidths (UWB); (2) an opening of 7 GHz of unlicensed spectrum at millimeter-wave frequencies (around 60 GHz) where oxygen absorption limits long-distance interference; (3) an overlay approach based on avoidance of higher-priority users through the use of spectrum sensing (cognitive radios). The potential opening of these new spectra introduces new opportunities for vastly more wireless connectivity. As indicated in Table 1, these three radio system are (or should be) allowed to operate in 500 MHz or wider spectrum. Therefore, the design of high-throughput radios with 100 Mb/s to even 1 Gb/s data rates is achievable at moderate-to-low spectrum efficiencies. The power limitations and wireless channel propagation characteristics for these bands dictate the range capability which extends from 1 m to 10 km, so that a wide variety of communication modes can be supported with these three new wireless radio technologies.

This regulatory shift also has major implications on radio architectures since traditional narrowband radio design techniques are not applicable. Spectrum sharing required in UWB and CR over wide bands implies frequency agility and significant dynamic range improvements of radio front-ends. In addition, new radio functions are required which involve high sensitivity sensing and modulation schemes robust to strong interferers and low signal-to-noise regimes. Interference avoidance through operation at microwave frequencies

Table 1: Potential system-level specifications consistent with FCC regulations and IEEE standards where they exist. Cognitive radios* do not have an allocation at this time.

Systems	UWB radio (UWB)	60 GHz radio (60 GHz)	Cognitive radio* (CR)
Spectrum access	Underlay	Unlicensed	Overlay
Carrier	[0–1], [3–10] GHz	[57–64] GHz	[0–1], [3–10] GHz
Bandwidth	> 500 MHz	> 1 GHz	> 500 MHz
Data rates	100–500 Mb/s	> 1 Gb/s	~ 10–1000 Mb/s
Spectrum efficiency	~ 0.1–1 b/s/Hz	~ 1 b/s/Hz	~ 0.1–10 b/s/Hz
Range	1–10 m	~ 10 m	1 m–10 km

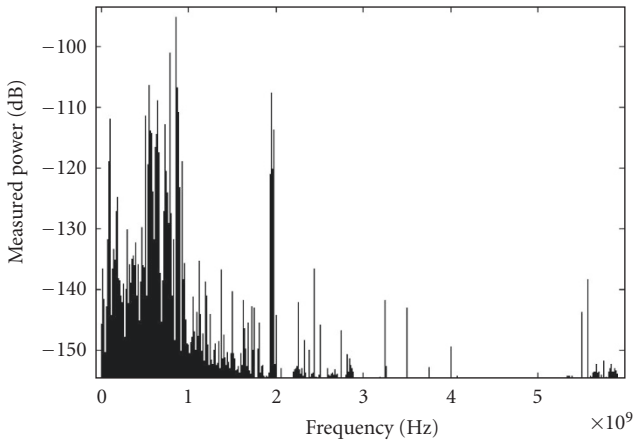


Figure 1: Spectrum utilization measurement (0–6 GHz).

introduces challenges in RF circuit implementation to ensure that the eventual solution is cost-effective.

In this paper, we present major opportunities and challenges of this new era in CMOS radio design, focusing on the three radio systems outlined in Table 1. Radio architectures which address the unique new requirements of these radios will be discussed including the analog and digital circuit partitioning, and the issues involved in antenna, RF, mixed-signal, and digital circuits.

2. UWB RADIOS

In 2002, the FCC released the use of ultra-wideband (UWB) transmission in several frequency bands (0–960 MHz, 3.1–10.6 GHz, and 22–29 GHz) with an effective isotropic radiation power (EIRP) below −41.3 dBm/MHz and requiring operation at larger than 500 MHz signal bandwidth [1]. The large bandwidth enables short-range high-data-rate communication and the possibility to perform high-resolution positioning. The new challenge for UWB radio implementation is to fully exploit the wideband nature for lower power and a less costly solution than by increasing the efficiency of narrowband techniques such as occurring in the standard 802.11n. A new opportunity using non-sinusoidal carriers, so-called impulse radios, has allowed designers to take a fundamentally new approach to radio architectures, signal processing techniques, and analog circuits. A low-complexity impulse radio architecture, together with its building blocks, will be given as an example of these new opportunities.

2.1. Low-complexity impulse radio architecture

The most discussed application of UWB is for short-range, high-speed, indoor communications. Two competing approaches have been introduced: one utilizing frequency-hopping OFDM and the other employing the impulse radio technique with direct-sequence coding. OFDM signaling strategy is essentially a scaled-up version of 802.11a/g system, which has the benefit of combating multipaths and potential power allocation for optimizing channel capacity. A major challenge of this approach is that the overall complexity is on the order of present 802.11 systems, which means that opportunities for dramatic cost and power reductions are unlikely. For example on the transmitter side, a wideband OFDM radio requires high-speed digital-to-analog converter, up-conversion mixers, oscillators, and power amplifier with linearity and peak-to-average ratio (PAR) constraints because of the multicarrier transmission [2]. On the other hand, an impulse radio simply uses a pulser to drive the antenna, and radiates a passband pulse shaped by the response of the wideband antenna and potential bandpass filters, as shown in Figure 2. The most popular modulation schemes using this approach are antipodal signaling or pulse-position modulation which have dramatically reduced linearity requirements at the expense of increased timing sensitivity.

The high-level schematic of an impulse radio architecture shown in Figure 2 shows the potential reduction in the complexity on the receiver side. Instead of the conventional heterodyne topology utilizing one or two mixing stages to downconvert the passband signal, the proposed receiver directly subsamples the incoming signal after amplification. This is accomplished by sampling at a rate below the Nyquist rate of the RF signal, but at or above the Nyquist rate of the data itself. The sampled and digitally converted data are processed by an optimized digital matched filter for optimal detection. The proposed system avoids wideband analog processing with increased digital processing, which results in a more efficient solution than conventional UWB implementations which have typically adopted a direct-conversion architecture [3–6] that results in significant increases in power dissipation.

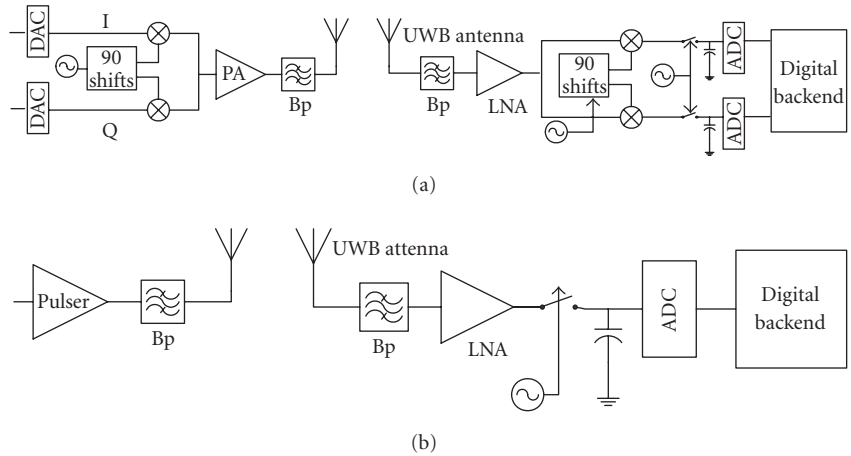


Figure 2: Transceiver of (a) one-stage heterodyne for OFDM approach, (b) proposed subsampling impulse radio.

2.2. UWB impulse radio frontend

2.2.1. Circuit modeling methodology for UWB small antennas

Ideally, the design of UWB antennas should satisfy several requirements: broad impedance bandwidth, high radiation efficiency, small size, omnidirectional radiation pattern, and broad radiation pattern bandwidth. These properties are generally strong functions of the antenna electrical size, and they are particularly challenging for the 0–1 GHz band, which is particularly interesting because of its good material penetration properties. The ability to design circuits that can provide efficient power transfer into the antenna (a good impedance match) and have an antenna pattern that is waveform omnidirectional is strongly dependent on the antenna size relative to the wavelength over the bandwidth of interest. For antennas that are electrically small, the impedance match is difficult to maintain, but the actual radiation pattern is almost constant over frequency; for antennas operating close to the first resonant frequency, the impedance match is good and the radiation pattern is only a weak function of frequency; however for antennas operating well above the first resonant frequency, while the impedance match is good, the radiation pattern changes rapidly with frequency. UWB antenna design is thus about designing the antenna around the first resonant frequency to achieve simultaneous impedance matching and constant radiation pattern over a wide bandwidth. The state-of-the-art UWB antennas report up to 4 : 1 impedance bandwidth but less than 3 : 1 bandwidth meeting both impedance and radiation pattern requirements [7–10]. Due to the limited impedance matching bandwidth, it is expected that the antenna impedance will deviate from 50 Ω, and will contribute waveform dispersion at both the transmitter and the receiver. How to capture the waveform dispersion, model the antenna impedance, and design the corresponding interface circuitry thus imposes a significant challenge in a UWB front-end design. A circuit modeling methodology that bridges the gap between UWB antenna and circuit design is thus necessary.

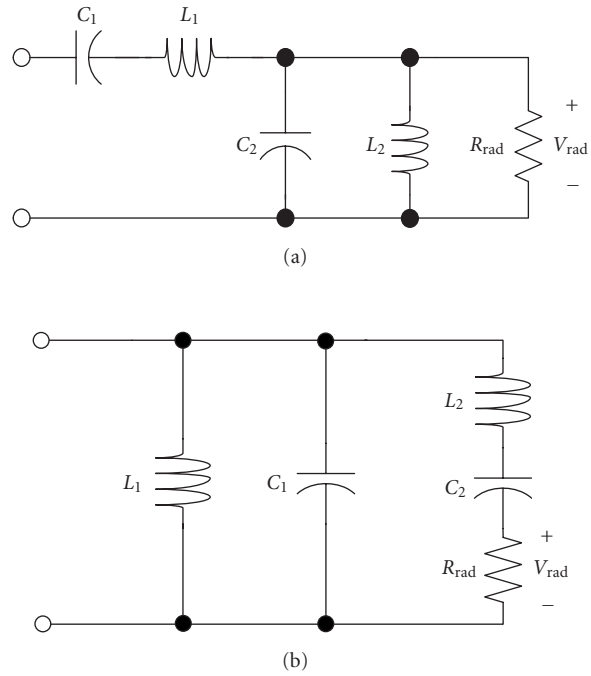


Figure 3: Degenerated Foster canonical forms for (a) electric antennas, and (b) magnetic antennas.

Generally, antennas are linear, passive elements and their input impedances can be represented by Foster canonical forms [11]. For UWB antennas of interest, one operates the antennas in the regime that their radiation pattern is constant with frequency, that is, below the second resonant frequency, so the Foster canonical forms can be degenerated to that shown in Figure 3. Figure 3(a) models electric antennas like dipoles and monopoles, and Figure 3(b) models magnetic antennas like loop antennas. The circuit models can be thought of as a load resistor R_{rad} with an LC bandpass filter in the front.

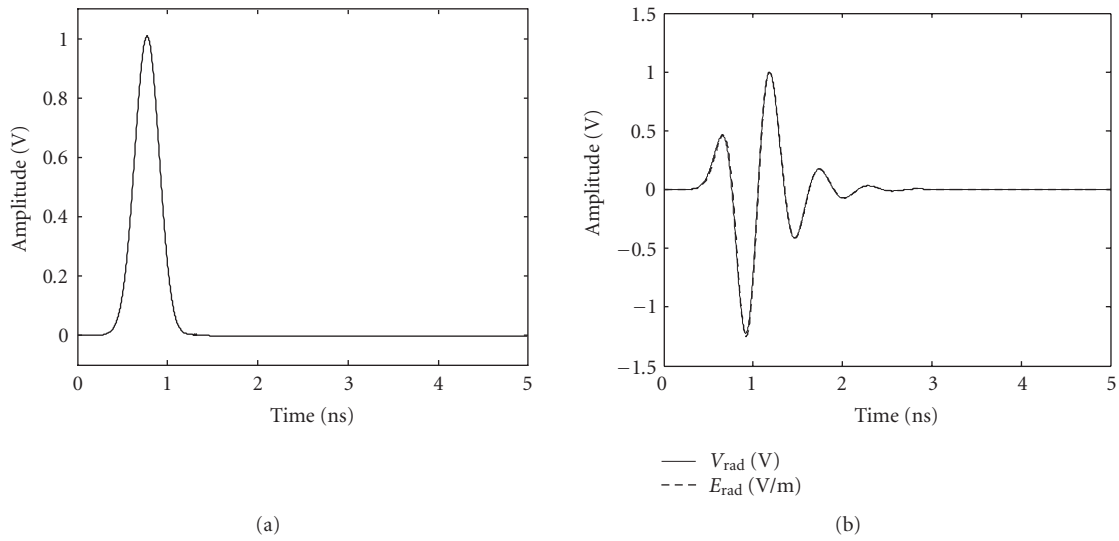


Figure 4: Time-domain waveforms of the 6 cm dipole antenna: (a) source voltage waveform with −10 dB bandwidth DC-2 GHz; (b) normalized V_{rad} from SPICE and E_{rad} ($\theta = 90^o$) from XFDTD.

The advantage of being waveform-omnidirectional, for which the waveforms of the radiated E-fields propagating in all directions are the same and thus differ only in magnitude, allows a simple antenna model to be built, which can be simulated on highly efficient circuit simulator instead of full electromagnetic simulation.

An example is given on modeling a dipole antenna. By fitting the input impedance of the circuit in Figure 3(a) to that of a 6 cm dipole antenna from FDTD simulation [12] using an optimization tool, we obtain $C_1 = 0.68$ pF, $L_1 = 1.24$ nH, $C_2 = 0.64$ pF, $L_2 = 4.91$ nH, and $R_{rad} = 187\,\Omega$. The resulting impedances from SPICE and FDTD match very well up to 5 GHz, which is almost twice the first resonant frequency. A 0.6-nanosecond-wide Gaussian voltage waveform is then sent into the antenna through a 50 Ω resistor (Figure 4(a)), and the voltage waveform V_{rad} and the far-zone E-field at $\theta = 90^\circ$ at 1 m away from the antenna are derived in SPICE and FDTD, respectively. After scaling and time shifting, Figure 4(b) shows that the two normalized waveforms match well indicating the effectiveness of the model.

2.2.2. Design of UWB pulse generator

In the past, UWB pulses were generated by circuits using exotic devices such as GaAs photoconductive switches, step-recovery diodes (SRD), tunnel diodes, or avalanche transistors. With the increased performance of scaled CMOS device size keeping scaling down and the device f_T enhanced, it is now possible to implement subnanosecond pulse generators using existing CMOS technologies and integrate it with other circuit blocks on a chip.

Ideally, after the antenna transfer function is derived as discussed in the previous section, a waveform meeting the FCC spectral mask can be generated by driving the antenna with the deconvolved waveform. The traditional way of doing this is to implement a linear power amplifier preceded by a high-speed digital-to-analog converter (DAC) with high resolution. However, high-performance DACs require significant power, and since the UWB transmitter is regulated to sub-mW power levels, it will lead to very poor power efficiency. An alternative is to use simple circuitry generating square pulses (similar to a 1-bit DAC) and filter them before the antenna. Figure 5 shows the proposed 2-PAM/PPM UWB transmitter that generates pulses below 960 MHz. A four-transistor balanced H-bridge driver is used to implement the voltage source. An off-chip filter/matching network helps to shape the waveform before it reaches the antenna. The H-bridge is driven by a predriver, which is further triggered by a timing circuitry. If a digital bit "1" is meant to be sent, transistors M_{P2} and M_{N1} are first turned on. A current will flow from Vdd through M_{P2} to the antenna, and through M_{N1} to ground. V_1 is raised immediately to Vdd, and V_2 is pulled down to 0. The differential output voltage of the H-bridge ($V\text{out} = V_1 - V_2$) is thus a rising step from 0 to Vdd. In the second half of the period, transistor M_{P2} is turned off and M_{N2} is turned on. V_1 then drops immediately to 0. The differential output voltage is thus a falling step from Vdd to 0. A rectangular pulse with magnitude equal to Vdd and pulse width equal to the interval between the switched-on times of M_{P2} and M_{N2} is formed. All the transistors are turned off by the end of the period. In contrast, if a digital bit "0" is meant to be transmitted, transistors M_{P1} and M_{N2} are first turned on, followed by the turn on of M_{N1}. A negative differential rectangular pulse can then be formed.

2.2.3. Design of UWB low-noise amplifier

Since the LNA is the circuit block that connects to the receiving antenna, its impedance will affect the waveform

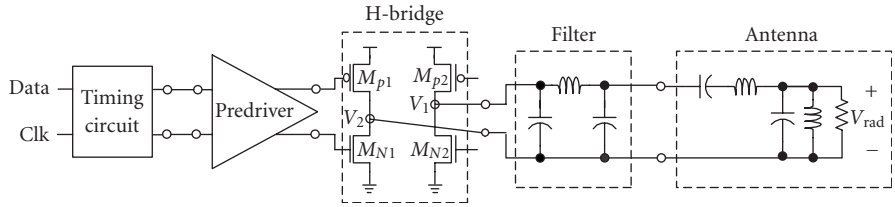


Figure 5: A CMOS pulse generator driving an electric antenna.

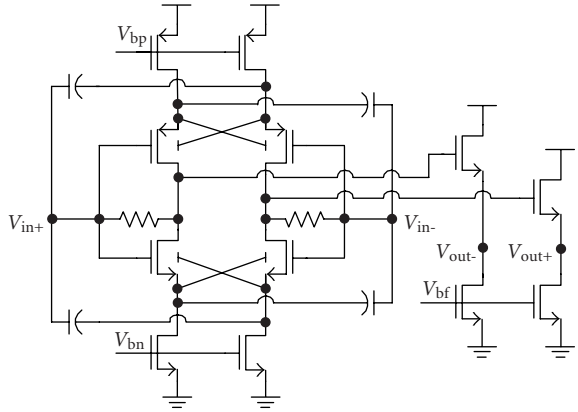


Figure 6: The < 1 GHz shunt-feedback/common-gate hybrid LNA.

dispersion. Also, if off-chip filters are to be used for band limiting, 50-ohm matching is desirable.

Since the in-band interference of UWB systems is much greater than the ambient noise, noise figure requirements can be relaxed to achieve lower power. A sub-mW UWB CMOS LNA has been proposed for the <1 GHz applications (Figure 6). By combining the shunt-feedback and common-gate amplifiers differentially, the amplifier achieves 13 dB of gain and a 3.6 dB of noise figure while consuming only 0.72 mW of power from a 1.2 V supply using a 0.13 μm CMOS technology [13].

2.3. Subsampling

After the antenna and LNA and any filters, impulses are sampled and detected digitally. But, short impulses require high-speed A/D conversion, and speed requirements for impulses in 3–10 GHz band are prohibitively large. One approach to reduce the sampling speed is to perform subsampling of a passband impulse by sampling at twice the signal bandwidth instead of the maximum signal frequency. For a bandlimited signal within F_l and F_h, the sampling frequency F_s along with F_l and F_h can be carefully chosen without aliasing the sampled spectrum [14]. For example, if the lower- or upper-frequency bound, that is, F_l and F_h, is a nonnegative integer multiple of the signal bandwidth B, the signal aliasing can be avoided at the minimal uniform sampling rate, $2B$,

$$F_l = n \cdot (F_h - F_l) = n \cdot B, \quad n \in \mathrm{N}. \tag{1}$$

An under-sampling ratio K is defined as,$\lfloor F_h/2B \rfloor$, the largest integer but smaller than $F_h/2B$. This ratio is a good indication of the amount of the aliasing effect.

The drawback of performing subsampling is noise folding, which is proportional to the ratio of the bandwidth center frequency to the signal bandwidth. For example, a UWB system centered around 4 GHz with a 1 GHz bandwidth has a subsampling ratio which only needs to be about 4-5. In addition, the wide signal band will contain substantial in-band ambient interference and noise, which the subsequent baseband processing must be designed to accommodate. This results in a relaxed SNR requirement due to noise folding. Simultaneously, the bandpass filtering requirement is also largely reduced by the much lower filter Q, simplifying the integration in a CMOS implementation. Finally, the relatively lower ADC resolution reduces the sampling clock jitter requirement.

A critical issue in the design is that the architecture is very sensitive to sampling offset, since a filter matched to the received pulse waveform is the optimal receiver. In Figure 7, the original passband signal is shown in the upper left corner along with subsampled versions with different offsets. These offsets can be introduced by frequency mismatch between the Tx and Rx oscillators or simply by small changes in the pulse arrival times. The sampled waveform will change dramatically due to this sampling offset, which will result in severe deterioration of the SNR of receive matched filter outputs.

2.4. Digital signal processing for impulse detection

A solution for sampling offset correction makes use of analytic signal processing as shown in Figure 8. This approach indicates a new opportunity in signal processing architectures for this type of radio. The sampling-offset problem arises because the received signals are treated as real-valued pulses, which would also arise in a sinusoidal radio if both I and Q signals were not used in the subsequent demodulation. While creating separate I and Q signals in a narrowband system can be accomplished by simply mixing with a 90-degree phase-shifted local oscillator, it requires the use of a Hilbert transformer for a wideband time-domain signal as given by $y(t) = s(t) + j * \hat{s}(t)$, where $\hat{s}(t) = s(t) * h_{\mathrm{Hilbert}}(t)$ is the Hilbert transform of the incoming (subsampled) signal, $s(t)$. $y(t)$ is the two-component analytic signal corresponding to the wideband I and Q paths, which are orthogonal to each other. As sampling offset varies, the signal energy

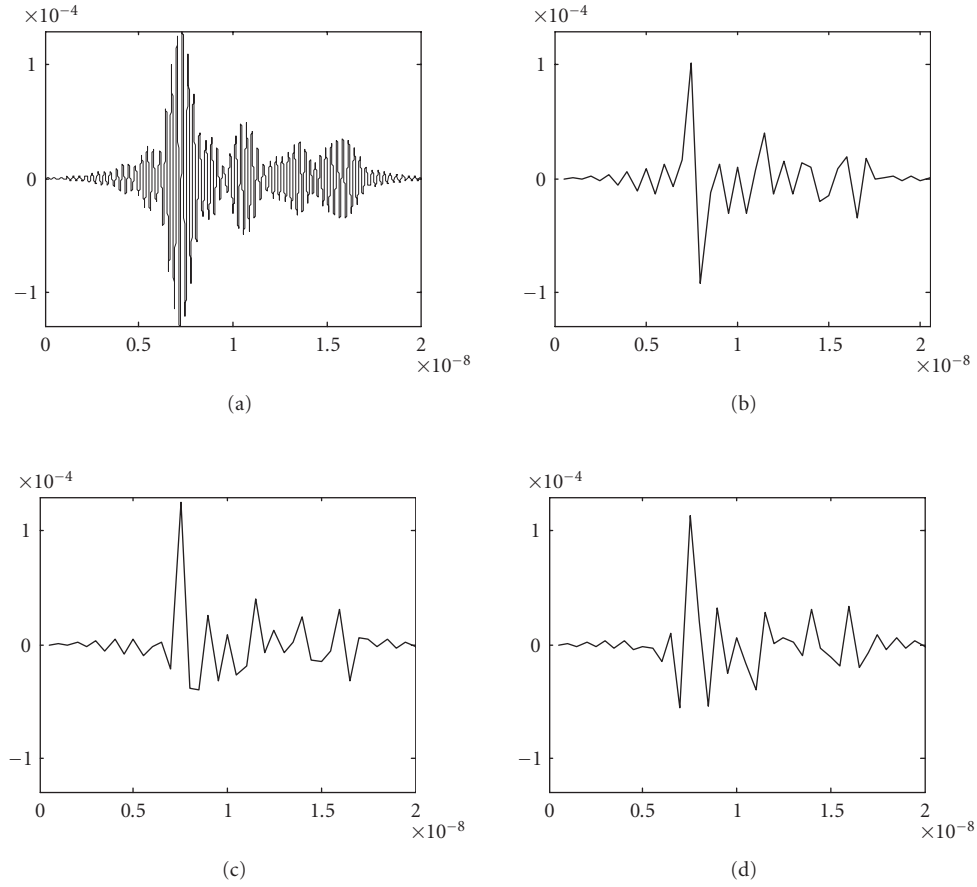


Figure 7: Pulse waveform with sampling offsets of (a) bandlimited pulse; (b) 0 *Ts*; (c) 0.05 *Ts*; (d) 0.1 *Ts*.

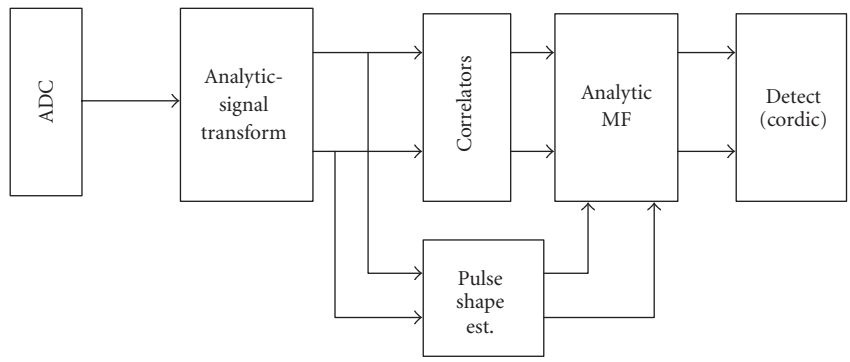


Figure 8: Digital backend block diagram utilizing analytic signal processing.

moves between the signal and its Hilbert transformed basis and a complex matched filter will then retain an offset-independent output.

The results can be explained from Figure 9, where the analytic matched filter outputs are plotted on Euler coordinates. 10 000 Monte Carlo experiments were simulated with and without a signal. Since an offset of just 5% of the sampling period rotates the complex signal about 30 degrees, a real-valued matched filter would have a substantially reduced signal-to-noise ratio, since it is essentially the projection onto the real axis which reduces the distance between noise and the filter output. An analytic filter on the other hand would provide the maximum distance to the noise which is present.

The reason why timing sensitivity is particularly an important problem for subsampling can be understood by the phase-shift term, $\exp(-2\pi kTo/Ts)$. The rotation angle is proportional to the ratio of To/T, and the undersampling ratio K. The Euclidean distance between the two constellations remains about the same, as opposed to the real-axis projection going to zero when the signal energy resides in

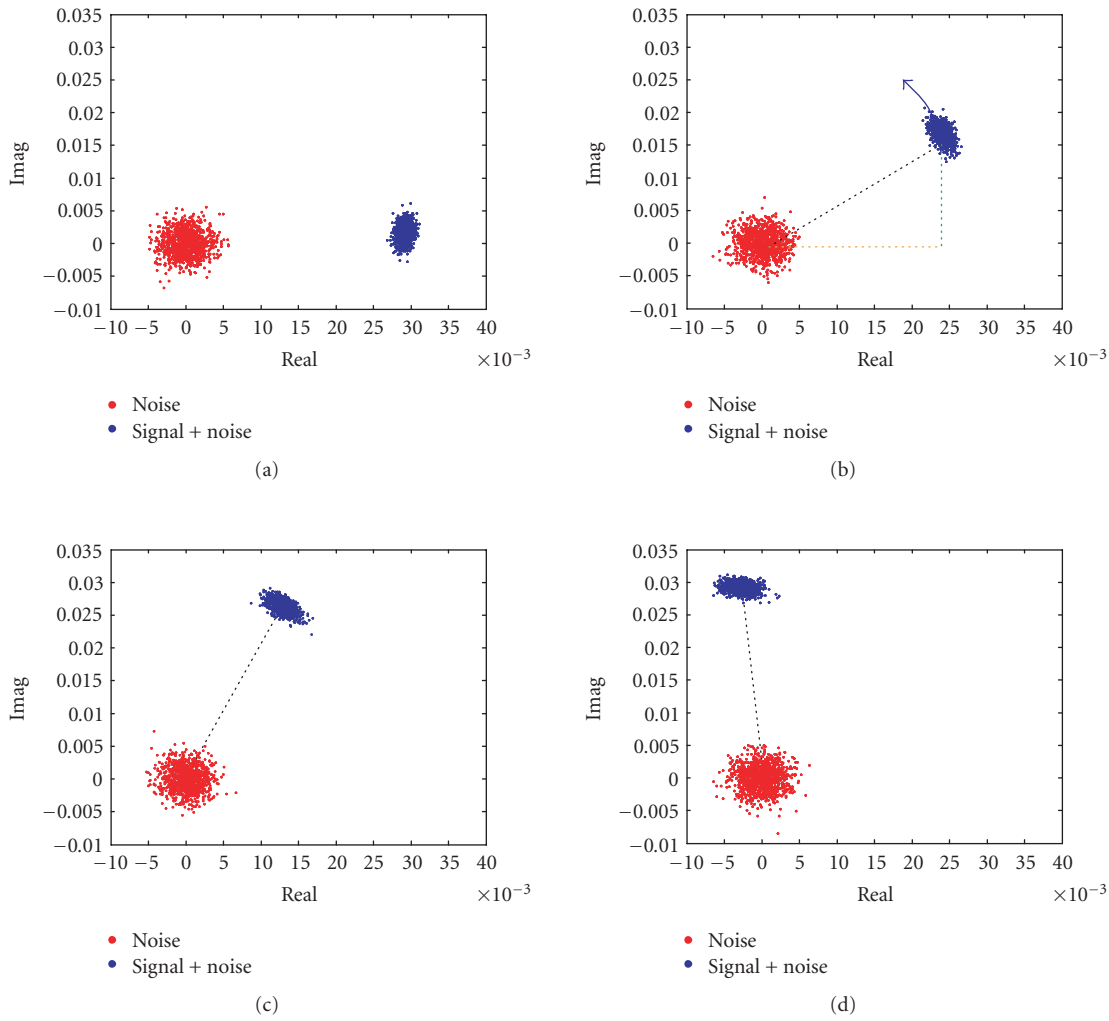


Figure 9: Plots of analytic matched filter outputs corresponding to $\{0, 5, 10, 15\}$% of Ts timing offset: (a) 0 Ts; (b) 0.05 Ts; (c) 0.1 Ts; (d) 0.15 Ts.

imaginary component. Thus, the magnitude of the analytic signal avoids nulls with respect to timing offset. The Hilbert transformers can be implemented in an FIR or fast Fourier transform (FFT).

While for the purpose of synchronization or data recovery, the timing sensitivity should be kept as small as possible, a high sensitivity implies increased time resolution for the system. Therefore, the proposed radio architecture can also be used for precision ranging/locationing applications. In the example, analyzed here, a 90-degree phase shift translates to a one-inch locationing accuracy.

3. 60 GHZ RADIOS

The FCC has allocated the 57–64 GHz band for general unlicensed use in the United States, and with the availability of 7 GHz of unlicensed spectrum around 60 GHz, there is growing interest in using this resource for new consumer applications requiring very high-data-rate wireless transmission. Furthermore, there is the likelihood of the development of a "worldwide" 60 GHz band, as both Europe and Japan are also in the process of allocating multi-GHz unlicensed bands at 60 GHz.

The 60 GHz band is well suited to high-data-rate indoor wireless communications. The sheer amount of usable bandwidth enables data capacities well in excess of the bandwidth-constrained 2.4 GHz and 5 GHz bands. Additionally, due to the oxygen absorption at 60 GHz, the FCC regulations allow for up to 40 dBm EIRP transmit power, which is significantly higher than what is available for the other WLAN/WPAN standards. The wide bandwidth and high allowable transmit power at 60 GHz enable multi-Gb/s wireless transmission over typical indoor distances (~10 m). However, several key issues present significant obstacles to the widespread adoption and several of the key challenges and relevant recent research progress will be discussed in the following sections.

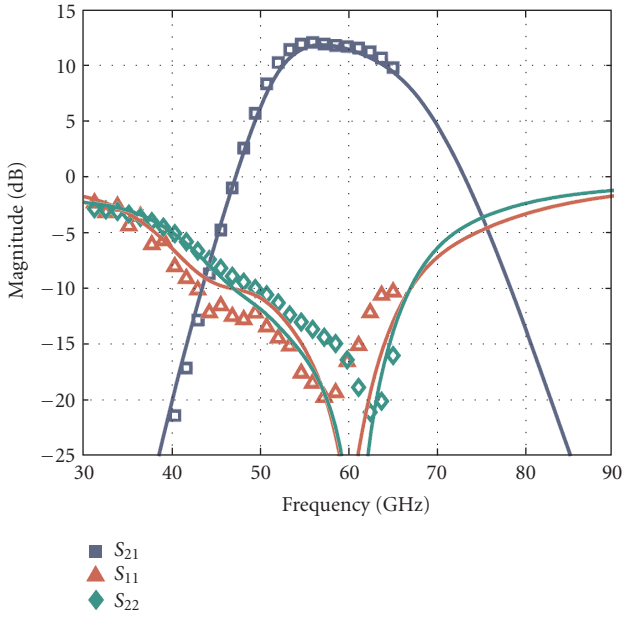


Figure 10: Measurements and predicted results of a 130 nm CMOS amplifier [16], measured (symbols) and simulated (lines) S-parameters.

3.1. 60 GHz CMOS microwave circuits

Historically, functional 60 GHz electronics components were only feasible in exotic III/V compound semiconductors [15]. In order to achieve widespread adoption of 60 GHz technology, it is necessary to implement these circuits in a low-cost technology such as CMOS or SiGe. Furthermore, development of silicon-based 60 GHz technology allows integration of complex digital functionality along with the microwave circuitry, thus enabling full SoC integration and further system-level cost reductions. Recent research has demonstrated that 60 GHz amplifiers can be designed and fabricated in 130 nm bulk "digital" CMOS [16]. Moreover, by utilizing a rigorous modeling and measurement methodology, highly predictable circuits can be designed. As shown in Figure 10, measured results for a 60 GHz amplifier designed in 130 nm CMOS match exceptionally well simulation results over the entire frequency band, thus opening up the opportunity for low-cost radios at 60 GHz. Therefore, 60 GHz circuitry has been demonstrated to be realizable in currently available CMOS technologies.

3.2. 60 GHz indoor wireless channel impairments

It is commonly believed that the 60 GHz indoor channel presents a challenging environment for high-data-rate wireless communications. The Friis path loss equation shows that, for equal antenna gains, path loss increases with the square of the carrier frequency. Therefore, 60 GHz communications must contend with an additional 22 dB of path loss when compared to an equivalent 5 GHz system. Also, the 60 GHz indoor channel suffers from typical multipath impairments with significant RMS delay spreads up to tens of nanoseconds, making Gb/s communications challenging.

However, 60 GHz antennas have a smaller form factor than 5 GHz antennas, as antenna dimensions are inversely proportional to carrier frequency. Therefore, more antennas can be placed within a fixed area, and the resultant antenna array can increase the antenna gain and help to direct the electromagnetic energy to the intended target. For example, a 60 GHz system with a 16-element antenna array has 3 dB gain over a 5 GHz omnidirectional system while occupying only 10% of the antenna area. Furthermore, the directive antenna pattern of a beamforming antenna array improves the channel multipath profile; by limiting the spatial extent of the transmitting and receiving antenna patterns to the dominant transmission path, the delay spread and Rician K-factor of an indoor wireless channel can be significantly improved [17]. This in turn opens up new opportunities for system and baseband design, as discussed in the next section.

3.3. Architectures for 60 GHz CMOS radios

Although 130 nm CMOS circuits are capable of operation at 60 GHz, the front-end circuits will inevitably have limited performance at these frequencies. In particular, the power amplifier (PA) output power and local oscillator (LO) phase noise will have a major impact on the achievable system performance. With 7 GHz of available bandwidth, it is possible to use spectrally inefficient schemes that are more tolerant of the limited performance of the CMOS mm-wave circuits. For example, constant-envelope modulation schemes minimize the linearity requirements on the PA, especially when compared to OFDM techniques typically used in low-GHz WLAN systems. Also, frequency-shift keying with low-order constellations is more robust to phase noise and receiver noise than the spectrally efficient modulation schemes typically used for low-GHz WLAN systems that are limited by the available bandwidth. Simulations of the effects of nonideal RF circuits on sample transient waveforms are shown in Figure 11. For these simulations, a nonlinear solid-state power amplifier (PA) model [18] with both AM/AM and AM/PM distortions and a local oscillator (LO) with a typical 60 GHz phase noise spectrum of −85 dBc/Hz at a 1 MHz offset [19] are assumed. The PA is driven at its 1 dB compression point to maximize its output power and efficiency; therefore, the linearity of the PA is significantly stressed by its operating conditions

The constellation plots in Figure 11 represent EVM plots of the signal at the transmitter output, *before* the effects of channel multipath, thermal noise, or nonidealities other than PA nonlinearity and LO phase noise are considered. As can be seen in the figure, complex modulation schemes with variable envelopes—such as 16-QAM and OFDM—are heavily distorted by the nonlinear behavior of the power amplifier and the phase noise from the LO. The resultant EVM of the OFDM transmitted signal is roughly 25%, corresponding to a transmit SNR of about 11 dB. With this level of EVM, performance at the receiver is significantly degraded. On the other hand, a constant-envelope scheme like minimum-shift

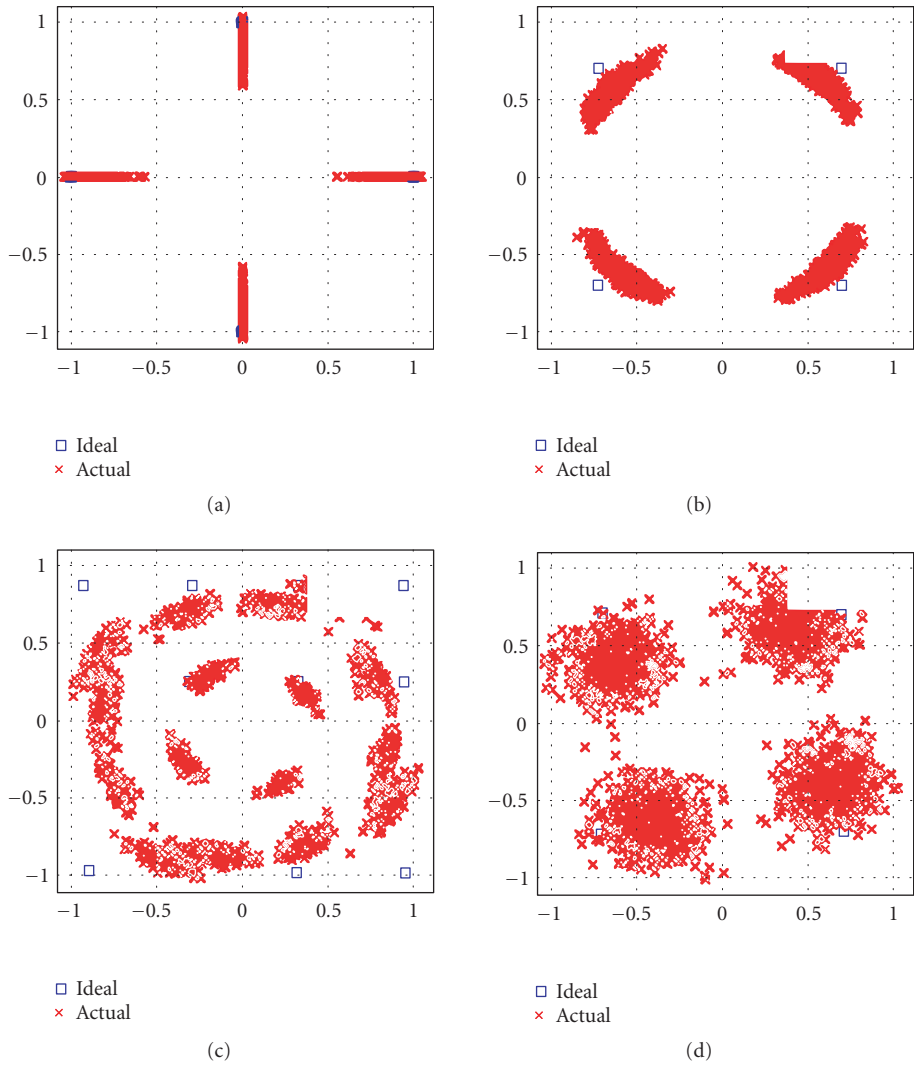


Figure 11: Effect of PA and LO nonidealities on signal constellations: (a) MSK constellation with nonideal VCO and PA; (b) QPSK constellation with nonideal VCO and PA; (c) QAM 16 constellation with nonideal VCO and PA; (d) OFDM, tone #5 with nonideal VCO and PA

keying (MSK) is far more resilient to these RF nonidealities. The EVM for the MSK transmitted signal shown is about 5%, corresponding to a transmit SNR of roughly 25 dB. As the transmitted waveform is only minimally degraded, receiver performance is not significantly affected. Therefore, single-carrier, constant-envelope signaling techniques—while spectrally inefficient—become the modulation scheme of choice in the presence of severe RF circuit nonidealities. Equalization of the received signal is still feasible in this system, as the directional pattern of the antenna array limits the resultant delay spread to just a few nanoseconds [17].

Baseband processing of such a wideband signal can have a large impact on the system complexity and power consumption of the mobile transceiver. In typical "mostly digital" wireless receivers or transmitters, the interface circuits (ADCs and DACs) are required to convert the signal with high resolution and operate at over twice the Nyquist rate of the signal. In multiple-antenna systems, where there may be several instantiations of the baseband circuitry, the aggregate power consumed by high-speed, high-resolution interface circuits may become prohibitively large.

If more of the signal processing is pushed into the analog domain, the resolution requirements of the interface circuits drop significantly. This hybrid approach is shown in Figure 12. Equalization and synchronization can be performed using a mixed-signal approach: maximum-likelihood estimation of the various parameter errors can be performed in the digital domain, where robust algorithms can be performed in digital architectures. These parameter errors are corrected in the analog domain, where simple high-speed analog circuits can properly condition the analog circuit prior to conversion.

The benefits of this approach can be best understood by comparing mixed-signal equalization to traditional digital

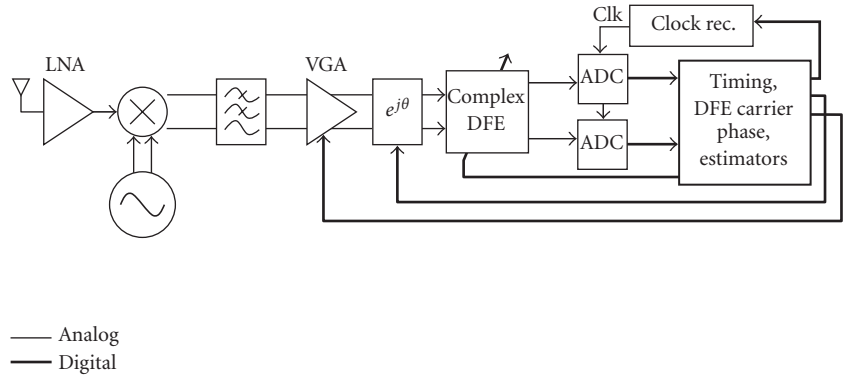


Figure 12: A mixed-signal baseband architecture for Gb/s transmission at 60 GHz.

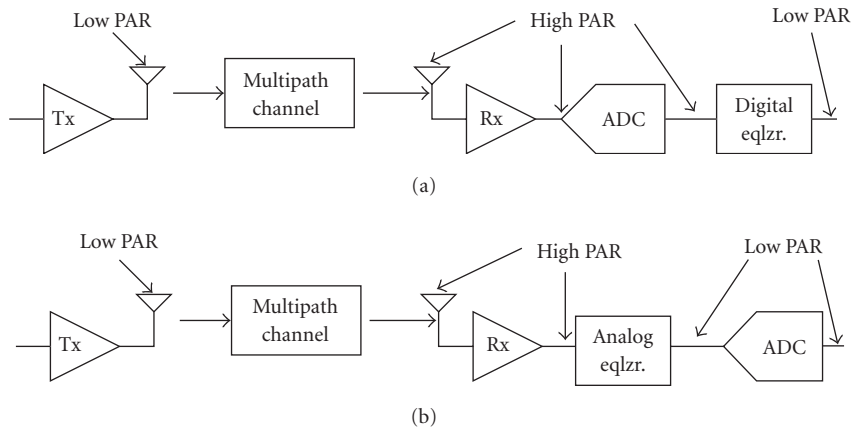


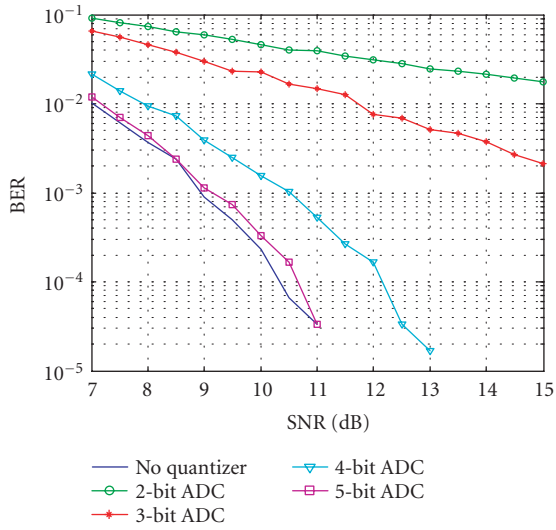
Figure 13: (a) Digital equalization requires more bits in the ADC; (b) mixed-signal equalization reduces the dynamic range of the signal seen at the ADC.

equalization. In the case of traditional digital equalization (Figure 13(a)), channel multipath results in an increase in the peak-to-average ratio (PAR) of the received signal. As a result, the ADC needs additional dynamic range (i.e., number of bits) in order to accommodate the multipath-distorted signal without degrading the received SNR. However, in a mixed-signal architecture (Figure 13(b)), the equalization step is performed in the analog domain prior to quantization. The mixed-signal equalizer is able to remove the multipath components of the signal, and hence reduces the PAR seen at the input at the ADC and as a result, a lower resolution ADC can be used.

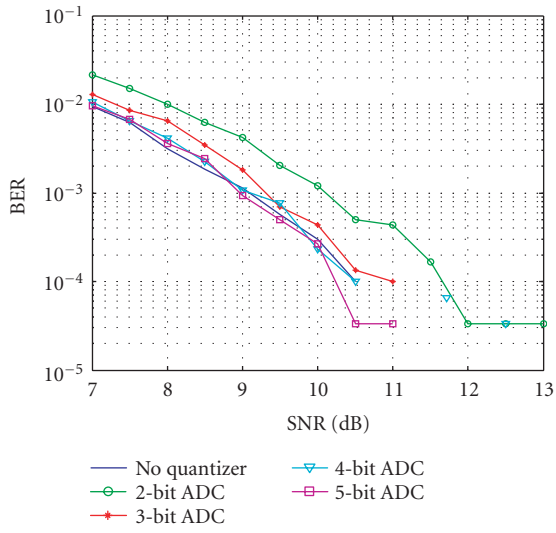
System simulations of a Gb/s MSK-based receiver using either digital equalization or mixed-signal equalization have been performed, and the results are presented in Figures 14(a) and 14(b). In these simulations, the channel is assumed to be Rician with a K-factor of 5 dB and an RMS delay spread of 15 nanoseconds. In addition, a 45-degree carrier phase offset is intentionally added at the transmitter, and perfect AGC is assumed. The equalizer is allowed to have 15 complex-valued taps in the feedback section; due to the specular nature of multipath reflections at 60 GHz [20], the feedforward portion of the DFE is not required. Figure 14(a) shows the performance of a receiver with a digital equalizer for various levels of ADC quantization. As can be seen in the figure, 5 bits of quantization are required in the digital equalization scheme in order to not suffer any receiver sensitivity loss; with the mixed-signal equalization scheme (Figure 14(b)), only 3 bits of quantization are required. Assuming that an extra bit of quantization is required as margin to cover AGC error or other system and circuit nonidealities, two 6-bit ADCs are required for the digital equalization scheme and two 4-bit ADCs are required for the mixed-signal scheme. State-of-the-art, 6-bit 2 Gs/s ADCs consume approximately 300 mW of power [21], whereas a 4-bit 2 Gs/s ADC currently in design is projected to consume under 15 mW of power. Therefore, power savings on the order of several hundreds of milliwatts can be achieved by utilizing a mixed-signal approach.

3.4. Mixed-signal baseband circuits for low-power, high-bandwidth receivers

In the mixed-signal architecture discussed in the prior section, carrier phase recovery and equalization are required



(a)



(b)

FIGURE 14: Receiver BER performance versus ADC bits for (a) digital equalization; $K = 5$ dB, trms= 15 perf. post equalizers, (b) mixed-signal equalization; $K = 5$ dB, trms= 15 perf mixed-sign equalizers.

prior to quantization by the ADC. Carrier phase recovery is required in order to account for phase and frequency offsets between the transmitter and receiver local oscillators. In order to perform analog carrier recovery, an analog phase rotator is required. An analog phase rotator is a block that takes an analog I/Q signal a s its input, and based on a control input θ, outputs an analog I/Q signal that is effectively rotated in the complex plane by the control angle. Therefore, we can implement an analog phase rotator as a network of variable-gain amplifiers as shown in Figure 15. Because the gain coefficient is either the sine or cosine of the control input θ, these VGAs require a gain range of -1 to $+1$. Each VGA in

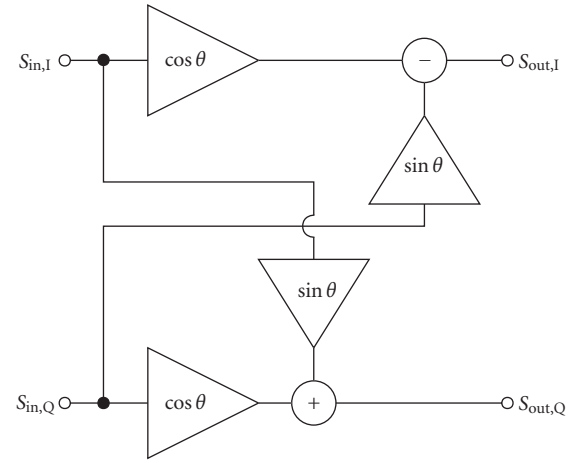


FIGURE 15: Block-level implementation of a complex phase rotator.

this phase shifter can be implemented as a doubly balanced Gilbert quad, as it can provide linear gain control between $+1$ and -1. The summation at the output of these VGAs is easily accomplished by utilizing the Gilbert quad circuit as a transconductor and performing the summation in the current domain. Furthermore, these Gilbert quads also provide the voltage-to-current conversion needed for the equalizer block that follows it.

Our proposed architecture for the analog phase rotator employs a digitally controlled tuning loop, as shown in Figure 16, to accurately tune each VGA to its proper gain. Switched-current DACs are used to set the ratio of the input current to the output current of the replica tuning circuit. Active feedback in the tuning circuit then sets the differential voltage applied to the Gilbert quad in order to accommodate the currents applied by the DACs, thus setting the gain of the quad circuit. This differential voltage is then applied to the primary VGAs in a master-slave fashion.

A mixed-signal decision-feedback equalizer (DFE) is required to remove the multipath components from the signal before it is quantized by the ADC. By performing this operation in the analog domain, the dynamic range of the signal at the input to the ADC is significantly reduced. A simplified block-level diagram of the DFE is shown in Figure 17. The input voltage-to-current conversion represented by the G_M cell at the input to the DFE is performed by the analog phase rotator block discussed above. The DFE works with current-based signals as it is more suitable to perform signal subtraction in the current domain than in the voltage domain. Each tap of the DFE is represented by a digitally switchable current cell, where the DFE switching pairs are controlled by past decisions ($d_{p,k}$ and $d_{n,k}$) in order to subtract the multipath components from the incoming signal. The magnitude of each tap coefficient is set by the magnitude of the tail current ($I_{T,k}$), which is in turn set by a digitally controlled DAC. The resultant output current is then applied to a transimpedance track-and-hold amplifier (not shown) that performs current-to-voltage conversion for the subsequent voltage-based ADC.

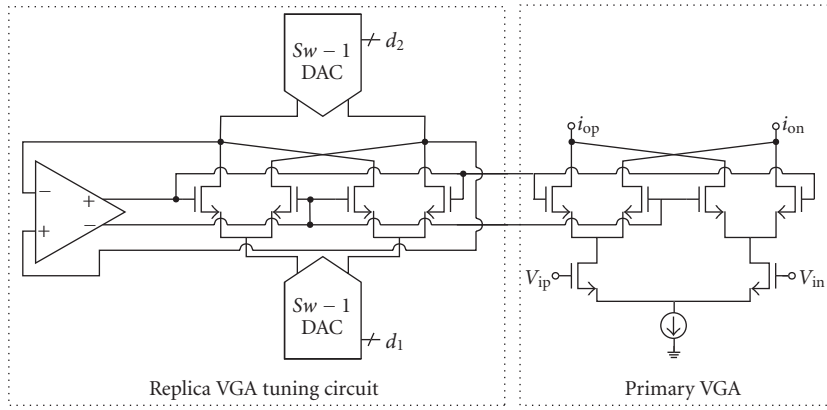


Figure 16: Gilbert quad VGA and tuning scheme for analog phase rotator.

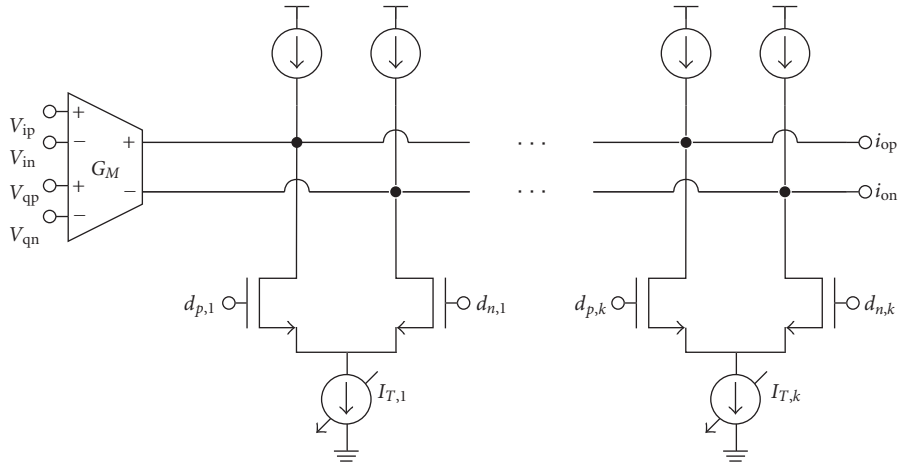


Figure 17: Simplified block diagram of a current-domain mixed-signal DFE.

4. COGNITIVE RADIOS

The FCC's original vision [22] was that cognitive radios may be used to implement opportunistic sharing by transmitting in licensed bands on a secondary noninterfering basis. Instead of regulating transmission parameters, cognitive radio communication would be strictly conditional on the reliable detection of an unoccupied spectrum, which is a receiver role. This requirement establishes a new type of functionality on the physical layer for spectrum sensing over all available degrees of freedom (time, frequency, and space) in order to identify modes currently available for transmission.

The importance of reliable detection of primary users is two-fold: (1) it ensures that cognitive radios would not interfere with primary users, which permits secondary use of their spectrum; (2) creates spectrum opportunities for capacity increase of cognitive networks. In order to realize this function, cognitive radios must have significantly better sensitivity and wideband frequency agility than conventional radios [23]. Therefore, an implementation of spectrum sensing requires novel designs of not only wideband RF/analog circuits, but also digital signal processing in order to meet such challenging requirements. In the next sections, we discuss the critical design issues in wideband sensing RF frontend and digital signal processing required to provide reliable detection of weak primary user's signals in the presence of large noise or interferers.

4.1. Wideband sensing receiver

Spectrum sensing requires the radio to receive a wideband signal through an RF frontend, sample it by high-speed ADCs conversion, and perform measurements for detection of primary users.

The new challenges are stringent requirement on RF front-end sensitivity for wideband signals and the ability to detect different primary signal types and received power levels. The wideband sensing requires a multi-GHz-speed ADC, which together with high resolution (of 12 or more bits) might be infeasible [24]. Therefore, reducing the strong in-band primary user's signals, which are of no interest, is necessary to receive and process weak signals with a realizable A/D.

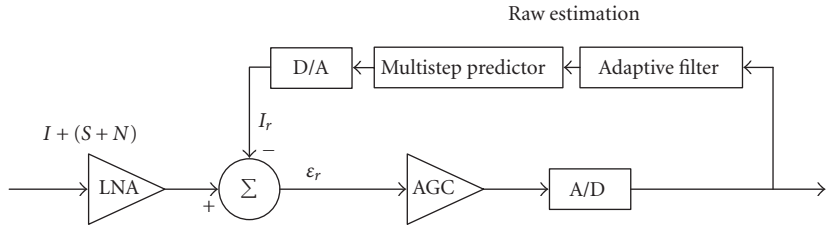


Figure 18: Feedback architecture for time-domain digitally assisted analog interference cancellation system.

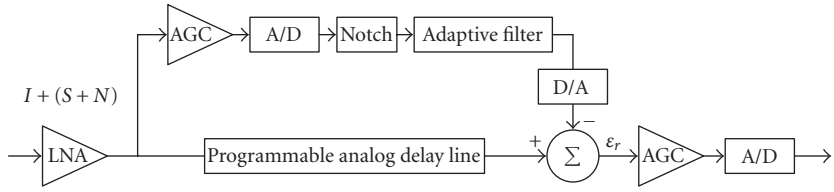


Figure 19: Feedforward architecture for time-domain digitally assisted analog interference cancellation system.

4.1.1. Active cancellation

One approach to remove the interfering signals could involve active cancellation in the time-domain, because in the situation in which the interfering signal is extremely strong, it is then possible to detect and duplicate the signal and then subtract it out before the A/D conversion process. Figure 18 illustrates an RF front-end architecture with digitally assisted active cancellation. Active cancellation is achieved through the use of an adaptive linear prediction filter and reconstruction D/A converter in a feedback loop.

The purpose of the loop is to subtract the interference signal, I caused by the strong primary (undesired) user. The feedback path (consisting of the adaptive filter, predictor, and D/A converter) extracts the primary user's signal for feedback cancellation. Because the A/D, D/A, and adaptive filter have intrinsic delays, a multistep predictor is needed in order to compensate for this delay. Upon loop convergence, the cancellation signal (I_r) roughly approximates the incoming interference (I), so that the dynamic range of the residue signal (E_r) is dramatically reduced, enabling the detection of the weak desired signal S.

There are several challenges in this feedback approach. Firstly, the adaptive filter used to regenerate the interference has a time-varying input signal and its estimation error due to noise, quantization, and prediction errors limits the performance of the interference cancellation. Secondly, since this is a closed-loop structure, it is difficult to guarantee its stability. Lastly, the key challenge in this approach is to perform analog subtraction in a closed loop with stringent timing constraints.

To overcome the limitations of the feedback architecture, an alternative feedforward architecture is proposed (Figure 19). The main idea of this approach is to use two low-resolution ADCs with N and M bits in order to achieve a high-resolution ADC of $N + M$ bits. It effectively behaves as a two-stage pipelined ADC, where the first-stage deploys sophisticated signal processing to provide reduced dynamic range to the second stage. The incoming signal goes through two paths, one branch deals with interference estimation and reconstruction, while the other is analog delay line to align the signals in two branches so that proper cancellation timing is achieved. The first stage ADC is the cancellation ADC and the ADC after subtraction is the residue ADC. The purpose of the notch filter is to remove the desired cognitive radio signal from the interference for improved estimation, and to avoid cancellation of the desired signals. The tradeoff between the number of bits in the cancellation ADC and residue ADC depends on the interference strength, that is, strong interference situations require more bits in cancellation ADC. While the timing constraints of the feedback loop are avoided by this architecture, it still requires matching of the latency through the two paths using an analog delay line.

4.1.2. Spatial filtering

An alternative approach for dynamic range reduction would be to filter the received signals in the spatial domain by using multiple-antennas. Through beamforming techniques, signals can be selectively received or suppressed using antenna arrays. However, multiple antenna processing must be done in the analog domain before the automatic gain control circuits that would properly amplify reduced dynamic range signal for the best utilization of the number of bits in the A/D converter.

The architecture of the wideband RF frontend which is enhanced with an antenna array for spatial filtering is shown in Figure 20. This architecture could be implemented as a phased antenna array where the antenna array coefficients are computed in digital domain and fed back to analog phase shifters which adjust the gains and phases of the antenna elements. The use of simple phase shifters is particularly attractive due to their very low latency needed for fast convergence of the desired array response.

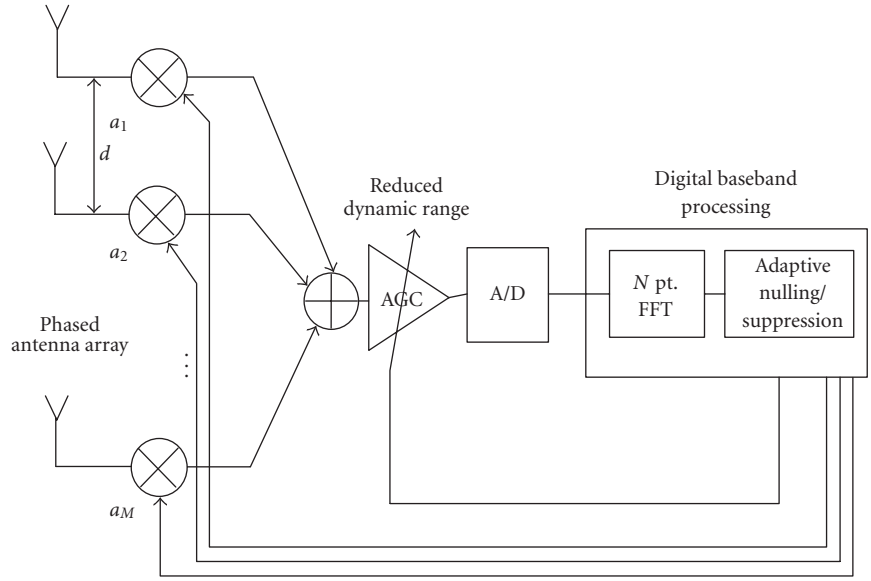


Figure 20: Wideband RF frontend with antenna array for spatial filtering.

A simple algorithm [25] for computation of optimal array coefficients could be derived by noticing that strong primary users occupy distinct frequency bands and directions of arrival. By applying an FFT on a wideband signal at the output of the A/D, a power profile in frequency domain is measured. In order to obtain the estimate of angle of arrivals, the antenna array coefficients must sweep through many directions. Given M antenna elements, any set of $K > M$ independent array coefficients is sufficient to obtain the estimation of spatial distribution. After identifying the frequency-spatial location of M strongest primary users through least-square estimation on these K measurements, array coefficients are set to attenuate their directions of arrivals.

Figure 21 shows the outlined algorithm performance for the case of two strong primary users whose power is 30–40 dB larger than average power in other frequency bands. After the optimal coefficients are applied, dynamic range reduces by approximately 22 dB (saving 3-4 bits in A/D converter) using a 4-element antenna array. Therefore, spatial filtering techniques could relax requirements for the implementation of RF wideband sensing frontend.

4.2. Signal processing for spectrum sensing

After reliable reception and sampling of a wideband signal, digital signal processing techniques should be utilized to further increase radio sensitivity by processing gain, and for primary user identification based on knowledge of the signal characteristics. The key issue in spectrum sensing is the detection of weak signals in noise with a very small probability of miss detection.

4.2.1. Matched filter and energy detector

A matched filter is the optimal detector in a sense that it can also demodulate signals due to coherent signal processing. The processing gain is linearly proportional to the number of samples N: $\mathrm{SNR}_{\mathrm{out}} = N \cdot \mathrm{SNR}_{\mathrm{in}}$. This gain is achievable under perfect frequency/timing synchronization and channel estimation required for coherent reception, but in low-SNR regimes heavily relies on the overhead of training pilot sequence. Therefore, a matched filter implementation complexity is prohibitively large since the cognitive radio would almost have to have a receiver for every primary user's system.

An energy detector is the suboptimal detector due to noncoherent signal processing, which only integrates squared samples. The processing gain is $\mathrm{SNR}_{\mathrm{out}} = N \cdot \mathrm{SNR}_{\mathrm{in}}^2$ which in case of a very small $\mathrm{SNR}_{\mathrm{in}}$ becomes significantly inferior to the matched filter due to quadratic scaling. The signal is detected by comparing the output of the energy detector with a threshold dependent on the estimated noise power. As a result, a small estimation error in the noise power causes significant performance loss of the energy detector. At the low SNRs of interest, the energy detector completely fails in the detection of weak signals. Even though the implementation simplicity (Figure 22) of the energy detector makes it a favorable candidate, the requirement to estimate the noise power of the actual RF transceiver within a fraction of a dB would be difficult to achieve. In practice, it would require a calibration of noise figure and gains of a wideband RF frontend across the whole frequency range.

In addition, an energy detector does not differentiate between modulated signals, noise, and interference. Since, it cannot recognize the interference, it cannot benefit from adaptive signal processing for cancelling the interferer. Furthermore, spectrum policy for using the band is constrained only to primary users, so a cognitive user should treat noise and other secondary users differently. Lastly, an energy detector does not work for spread-spectrum signals: direct-sequence and frequency-hopping signals, for which more sophisticated signal processing algorithms need to be devised.

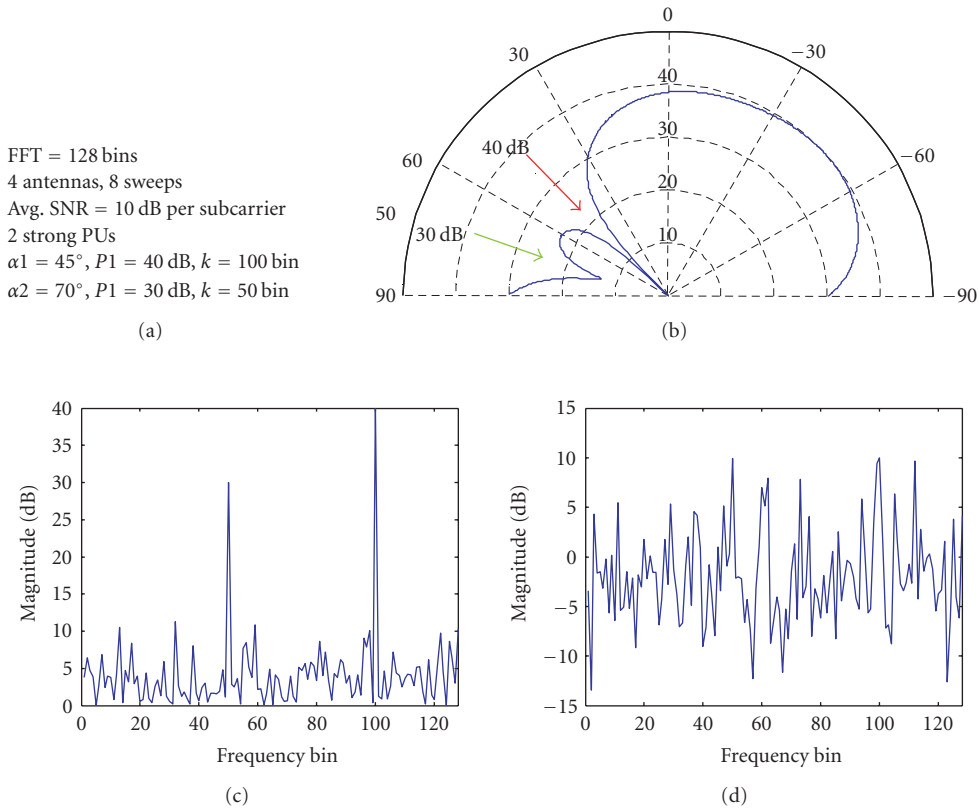


Figure 21: An example of dynamic range reduction using antenna arrays: (a) simulation parameters; (b) optimal array response; (c) large dynamic-range signal; (d) spatially filtered signal.

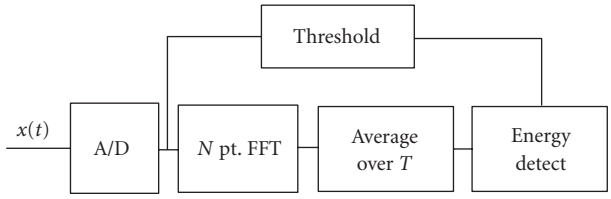


Figure 22: Implementation of an energy detector using Welch periodogram averaging.

4.2.2. *Cyclostationary feature detector*

Cyclostationary feature detectors have the ability to extract distinct features of modulated signals such as sine-wave carrier, symbol rate, and modulation type. These features are detected by analyzing a spectral correlation function that is a two-dimensional transform, in contrast with power-spectrum density being one-dimensional transform [26]. The main advantage of spectral correlation function is that it discriminates the noise energy from modulated signal energy. This property is a result of the fact that noise is a wide-sense stationary signal with no correlation, while modulated signals are cyclostationary with spectral correlation due to embedded redundancy of signal periodicities. Therefore, a cyclostationary feature detector is a better alternative than energy detector due to its robustness to unknown noise variance.

Implementation of a spectrum correlation function for cyclostationary feature detection is depicted in Figure 23. It can be designed as augmentation of the energy detector from Figure 22 with a single correlator block. Detected features are number of signals, their modulation types, symbol rates and presence of interferers. Figure 24 illustrates the advantages of cyclostationary detection versus energy detection for continuous phase 4-FSK modulated signals. Distinct pattern of 4-FSK modulation in a spectral correlation function is preserved even in low SNR $= -20$ dB while energy detector is limited by the large noise.

Its implementation complexity is increased by N^2 complex multiplications to perform the cross-correlation of the N-point FFT outputs, while the energy detector has the complexity of an N-point FFT.

5. CONCLUSION

The demand for wireless connectivity has pushed the regulatory agencies to be ever more aggressive in providing new ways to use spectra. The radio systems that are made possible by these new opportunities allow for new optimization at the architectural, circuit, and algorithm levels. Three of these

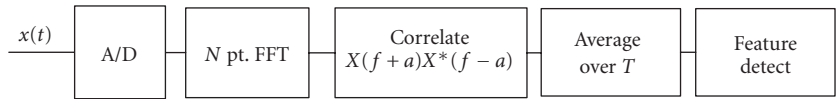


Figure 23: Implementation of a cyclostationary feature detector.

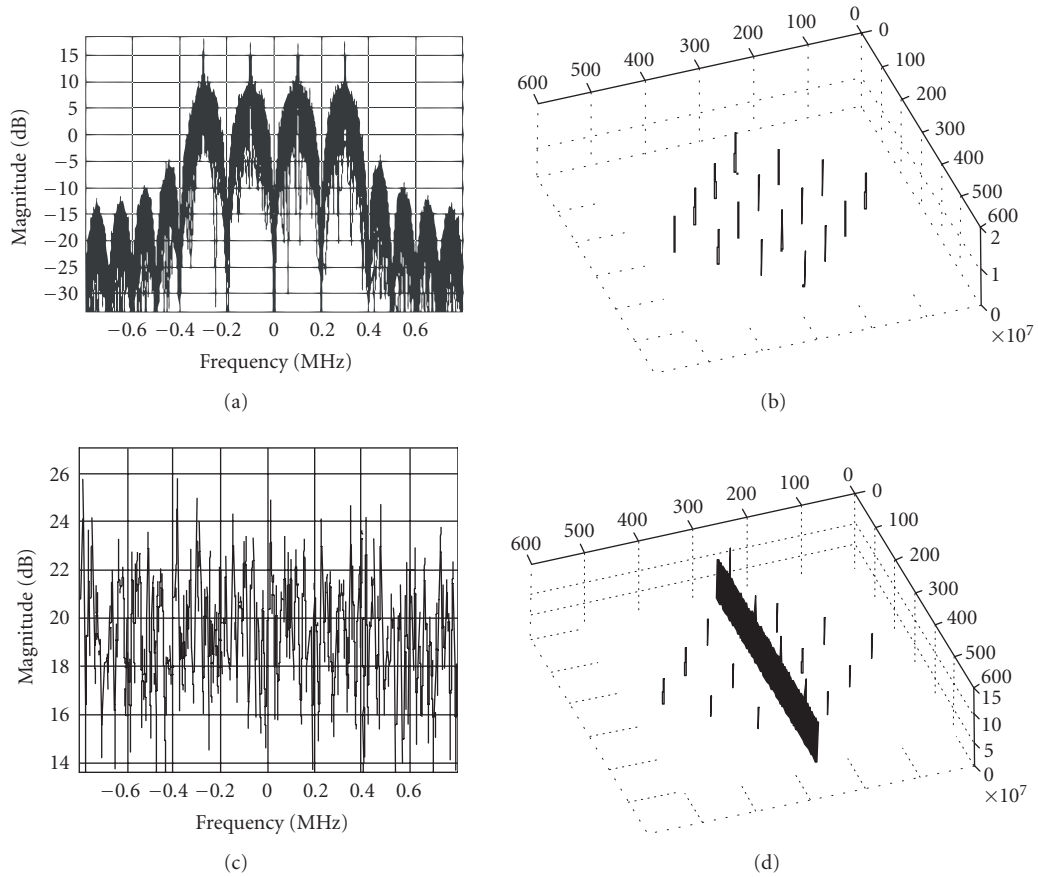


Figure 24: Detection of a continuous-phase 4-FSK using energy detection and cyclostationary feature detection. (a) PSD of 4-FSK SNR = 10 dB; (b) SCF of 4-FSK SNR = 10 dB; (c) PSD of 4-FSK SNR = −10 dB; (b) SCF of 4-FSK SNR = −20 dB.

new radio systems were discussed with some examples of solutions to the new challenges that are being posed. There are clearly further opportunities in all of these new approaches for designers to express their creativity, so it is an exciting time to be a radio designer and an architect.

ACKNOWLEDGEMENT

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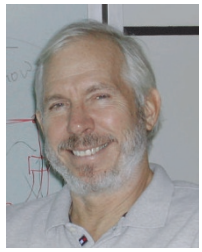

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