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Low complexity look up table based adaptive digital predistorter with low memory requirements

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Abstract

With the advent of spectrally efficient wireless communication systems employing modulation schemes with varying amplitude of the communication signal, linearization techniques for nonlinear microwave power amplifiers (PAs) have gained significant interest. In this article, a low complexity, direct-learning multilevel lookup table based adaptive digital predistortion technique has been proposed to linearize a PA. A loop delay compensation scheme has been used to achieve a significant reduction in convergence time and an improvement in linearization accuracy in the presence of an unknown loop delay. Compared with the conventional predistorters, the proposed technique shows fast adaptation speed which enables the predistorter to track time-varying PA nonlinearities.

1. Introduction

Power amplifiers (PAs) are important components in a communication system, but they are inherently nonlinear. The nonlinearity produces spectral re-growth, which leads to adjacent channel interference and violations of the out of band emission standards. It also causes in band distortion, which degrades the bit error rate and data throughput of the communication system. To reduce the nonlinearity, the PA can be backed off so that it operates within the linear portion of its operating region. However, newer transmission formats, such as wideband code division multiple access, have large fluctuations in their signal envelopes, i.e., high peak-to-average power ratios. This means that the PA needs to be backed off well below its maximum saturated output power in order to handle infrequent peaks, which result in very low efficiencies.

To maintain linearity and efficiency, one can apply linearization to the PA through several compensation techniques such as feedback, feed-forward, and digital predistortion (DPD). In feedback approach, part of the output power is fed back to control the input power. But, this method demands a high loop gain and a sufficient phase margin for stability [1-3]. On the other hand in feed-forward compensation, a suitable signal is added to the output signal for linearization. But in case of high power PAs a high power summing point can hardly be implemented. In DPD technique, the PA input signal is predistorted in such a manner that the overall system becomes approximately linear, as depicted in Figure 1.

DPD works entirely in the digital domain and is already in use in 2G systems. The techniques are mostly based on look up tables (LUTs) [4], using a memory-less characteristic of the PA. With large signal bandwidths as in 3G systems, memory effects become more pronounced [5]. Therefore, for such systems memory-less LUT approach will be of no use. Some of the noted work on LUT-based DPD can also be found in [6-8]. In this article, attention is focused on the development of an adaptive LUT-based DPD linearization technique which solve the linearization problem in an optimal way.

In the following sections, an adaptive DPD technique is modeled and simulated. The aim of this article is to develop a linearization technique which is less complex and requires less memory from FPGA implementation point of view.

In Section 2, the basic approach is described. In the last section, the simulation of the system and the computation of the LUT values have been reported.

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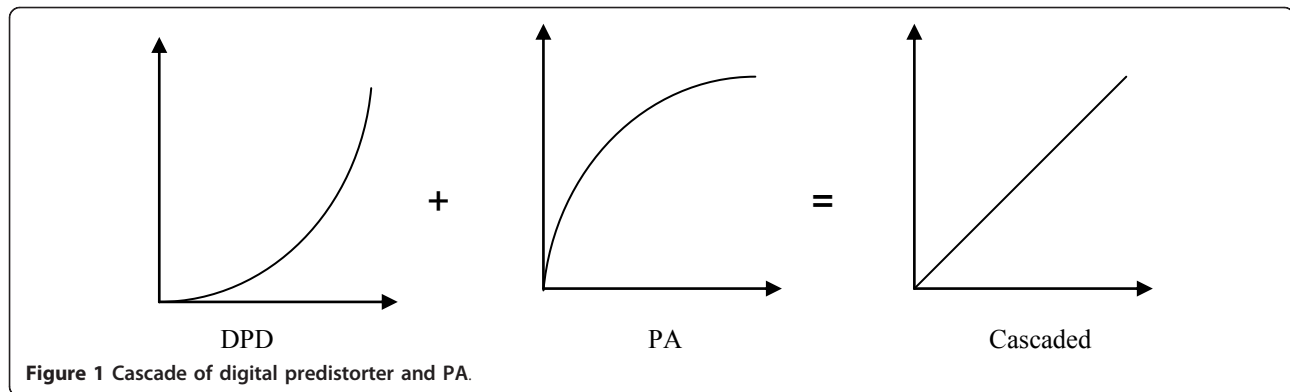Electronics and Communication Engineering Department, Thapar University, Patiala, India

Figure 1 Cascade of digital predistorter and PA.

2. Basic approach used in design of adaptive digital predistorter

LUT-based digital predistorters have low computational complexity, but they require significantly more memory space to store the model parameters than polynomial-based digital predistorters. Thus, LUT-based digital predistorters have slow convergence speed as compared to polynomial-based digital predistorters. Comparatively, evaluation of a polynomial function is more computationally complex than a simple memory LUT entry and compensation of higher orders of nonlinearity and memory effects requires a high order polynomial. For newer spectral efficiency transmission formats, a predistorter bandwidth of several tens of MHz might be required for implementation of these high order polynomials. In this article, a novel low complexity LUT-based adaptive digital predistorter with reduced memory requirements has been proposed by using interpolation and efficient spacing of table entries, which leads to low LUT requirement. The proposed adaptive digital predistorter has much higher convergence rate as compared to other LUT-based adaptive digital predistorters.

In the proposed design, polar LUT-based predistorter [9] has been used and is shown in Figure 2.

Functions $f_\rho(x)$ and $f_\theta(x)$ denote the nonlinear AM-AM and AM-PM distortions of PA. The polar predistorter consists of two LUTs that approximate the inverse function of the PA's amplitude distortion $h_\rho(x) = f_\rho^{-1}(x)$ and the phase compensation function $h_\theta(x) = -f_\theta(x)$.

For computing the error in determining $h_\rho(x)$ and $h_\theta(x)$, consider the nth entry of the amplitude LUT. For input amplitude, $x_i = x_n + \varepsilon_x$ with $0 < \varepsilon_x \le d_n$, where $d_n = x_{n+1} - x_n$ is the width of the nth interval, the output of the LUT predistorter will be $h_\rho(x_i) + \varepsilon_{h\rho}$. Because the calculation in error of $h_\rho(x)$ and $h_\theta(x)$ is similar. So, only derivation for calculating the error $\varepsilon_{h\rho}$ in determining $h_\rho(x)$ will be presented, and is as follows:

Let $h_\rho(x)$ be a doubly differentiable function that is evaluated at points (x_i, y_i) with $y_i = h_\rho(x_i)$, where $i \in 1,2,\ldots,N$. The closed-form expression of the interpolation error within the interval $[x_n, x_{n+1}]$ will be derived, for $1 < n < N$. Let us assume that the interval considered is small enough that $h_\rho(x)$ can be approximated by a second-order polynomial within the nth interval. This is equivalent to neglecting the error terms above the second-order term in a Taylor series expansion. Consequently, the second-order derivative of $h_\rho(x)$ can be
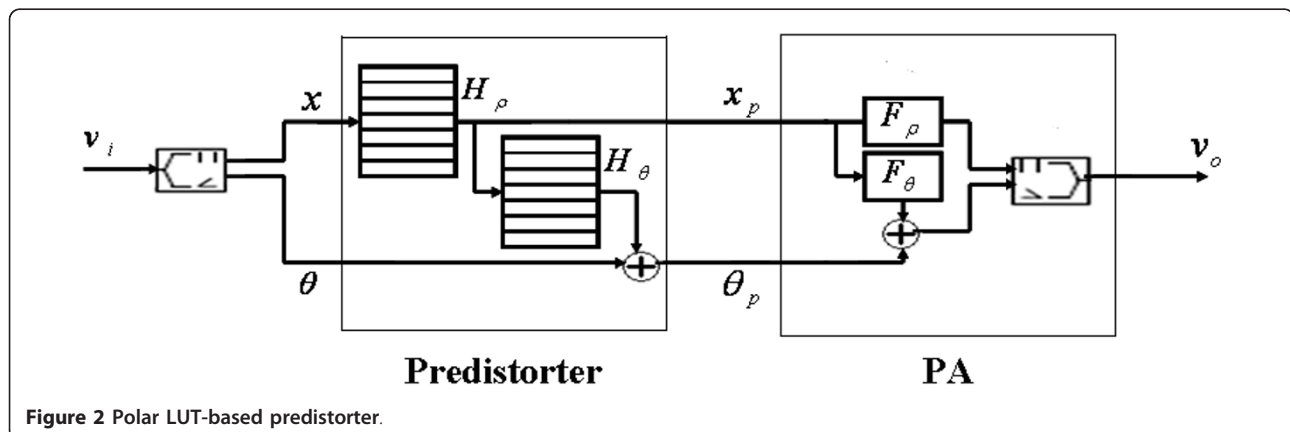

Figure 2 Polar LUT-based predistorter.

considered as a constant within the interval. The previous assumption is reasonable here since otherwise a linear approximation of f in that interval would yield a very inaccurate approximation. $h_\rho(x)$ is therefore given by

$$h_\rho(x) = \alpha x^2 + \beta x + \gamma \text{ for } x_n \le x \le x_{n+1} \tag{1}$$

After a few trivial algebraic manipulations, the coefficients α, β and γ can be calculated from the two reference points as functions of $h_\rho''(x), x_n, x_{n+1}, y_i, y_{n+1}$

$$\alpha = \frac{h_\rho''(x)}{2} \tag{2}$$

$$\beta = \frac{y_n - y_{n+1}}{x_n - x_{n+1}} - \frac{h_\rho''(x)}{2}(x_n + x_{n+1}) \tag{3}$$

$$\gamma = \frac{x_i \times y_{n+1} - x_{n+1} \times y_k}{x_i - x_{n+1}} - \frac{h_\rho''(x)}{2}(x_n \times x_{n+1}) \tag{4}$$

The linear approximation of $h_\rho(x)$ in the nth interval can be formulated as follows

$$\tilde{h}_\rho(x) = ax + b \tag{5}$$

where a and b can also be expressed as a function of $x_n, x_{i+1}, y_n, y_{n+1}$.

$$a = \frac{y_n - y_{n+1}}{x_n - x_{n+1}} \tag{6}$$

$$b = \frac{x_n \times y_{n+1} - x_{n+1} \times y_n}{x_n - x_{n+1}} \tag{7}$$

The interpolation error between $h_\rho(x)$ and $\tilde{h}_\rho(x)$ for $x_n < x < x_{n+1}$ can be calculated as follows

$$e_i(x) = h_\rho(x) - \tilde{h}_\rho(x) \tag{8}$$

Solving (8) using (1) to (7), we get

$$e_i(x) = \frac{h_\rho''(x)}{2}(x - x_n)(x - x_{n+1}) \tag{9}$$

Let ε_x be the deviation between x and x_n, and d_n the width of the nth interval

$$\varepsilon_x = x - x_n \tag{10}$$

and

$$d_n = x_{n+1} - x_n \tag{11}$$

The expression of the linear interpolation error can then be rewritten as follows

$$\varepsilon_{h\rho} = h_\rho''(x)\frac{\varepsilon_x(\varepsilon_x - d_n)}{2} \tag{12}$$

The amplitude at the output of the PA is

$$\begin{aligned} x_o &= f_\rho[h_\rho(x_i) + \varepsilon_{h\rho}] \\ &\approx f_\rho[h_\rho(x_i)] + \varepsilon_{h\rho}f_\rho'[h_\rho(x_i)] \\ &\approx x_i + \frac{h_\rho''(x)}{h_\rho'(x_i)}\frac{\varepsilon_x(\varepsilon_x - d_n)}{2}, \end{aligned} \tag{13}$$

Also the amplitude error measured at the PA's output can be expressed as $e_\rho = x_o - x_i$

$$= \frac{h_\rho''(x)}{h_\rho'(x_i)}\frac{\varepsilon_x(\varepsilon_x - d_n)}{2} \tag{14}$$

The output phase error can be expressed as

$$e_\theta = f_\rho''(x_i)\frac{\varepsilon_x(\varepsilon_x - d_n)}{2} \tag{15}$$

Assuming that the amplitude and phase errors to be very small, the output of the PA can be written as

$$\begin{aligned} v_o &= (x_i + e_x)e^{j(\theta_i + e_\theta)} \\ &\approx (x_i + e_x)\left[e^{j\theta_i} + e_\theta e^{j(\theta_i + \pi/2)}\right] \\ &\approx v_i + e_x e^{j\theta_i} + e_\theta x_i e^{j(\theta_i + \pi/2)} \end{aligned} \tag{16}$$

Thus the error at the output of the PA can be given by

$$\begin{aligned} e_o &= v_o - v_i \\ &\approx e_x e^{j\theta_i} + e_\theta x_i e^{j(\theta_i + \pi/2)} \end{aligned} \tag{17}$$

The residual error at the output of the PA consists of two terms resulting from the approximation errors in the amplitude and phase LUTs. These two error terms can be considered independent of each other to simplify the remaining calculations. The total noise contribution of the nth entry to the output SNR can be computed using the usual quantizer assumption [10] that ε_x is a random variable uniformly distributed in $[0, d_n]$. The mean-squared error (MSE) contribution of the nth entry of the amplitude table is

$$\begin{aligned} E\left[|e_\rho|^2\right] &= \frac{h_\rho''(x)^2}{4d_n h_\rho'(x_n)^2}\int_0^{d_n}\varepsilon^2(\varepsilon - d_n)^2 d\varepsilon \\ &= \frac{h_\rho''(x)^2}{120 h_\rho'(x_n)^2}d_n^4 \end{aligned} \tag{18}$$

Similarly, the contribution of the nth of the phase LUT to the total residual error is

$$E\left[\mid e_\theta \mid^2\right] \approx \frac{h_\theta''(x_n)^2}{120}x_n^2d_n^4 \qquad (19)$$

For an arbitrary LUT spacing achieved using a compander [10]$c(x)$, the LUT entry width is related to the compander by

$$d_n \approx \frac{1}{Nc'(x_n)}, \qquad (20)$$

where N is the LUT size and V is the maximum amplitude addressable by the LUT. For the special case of uniform spacing $c(x) = x$ and $d_n = 1/N$ is constant. Assuming that the number of LUT is large enough, the total residual distortion power at the PA output can be approximated as follows:

$$P_{dis} = P_\rho + P_\theta \qquad (21)$$

with

$$P_\rho = \frac{1}{120N^4}\int_0^1 \frac{h_\rho''(x)^2}{c'(x)^4h_\rho'(x)^2}p(x)dx \qquad (22)$$

$$P_\theta = \frac{1}{120N^4}\int_0^{\overline{A}} \frac{h_\theta''(x)^2}{c'(x)^4}x^2\widetilde{p}(x)dx \qquad (23)$$

where $p(x)$ is the probability density function (PDF) of the input amplitude and $\widetilde{p}(x)$ is the PDF of the predistorted amplitude of the input signal. Equations (22) and (23) show that the mean-squared amplitude and phase errors are inversely proportional to N^4, which is a much faster rate of decrease than [11], which results in a MSE that is inversely proportional to only N^2.

3. Proposed design

The block diagram shown in Figure 3 shows the simulation platform used in the proposed design.

This platform has been implemented using Agilent ADS software. Because, each block has been implemented at component level, so details of each component have not being given deliberately. The training signal is a tone having an increasing magnitude, i.e., a ramp. The tone is generated by uniformly increasing the amplitude of the in-phase and quadrature component of the complex baseband signal. The shape of training ramp is shown in Figure 4.

Only the rising portion of the ramp is used by the adaptation algorithm in the calculation of the predistortion function. The hold and trailing ramp portions are included to smooth the transition between power levels and minimize the impact of finite length filters on the latter part of the rising portion of the ramp. The early implementations of LUT predistorters were mainly based on uniform spacing in power to reduce the complexity of
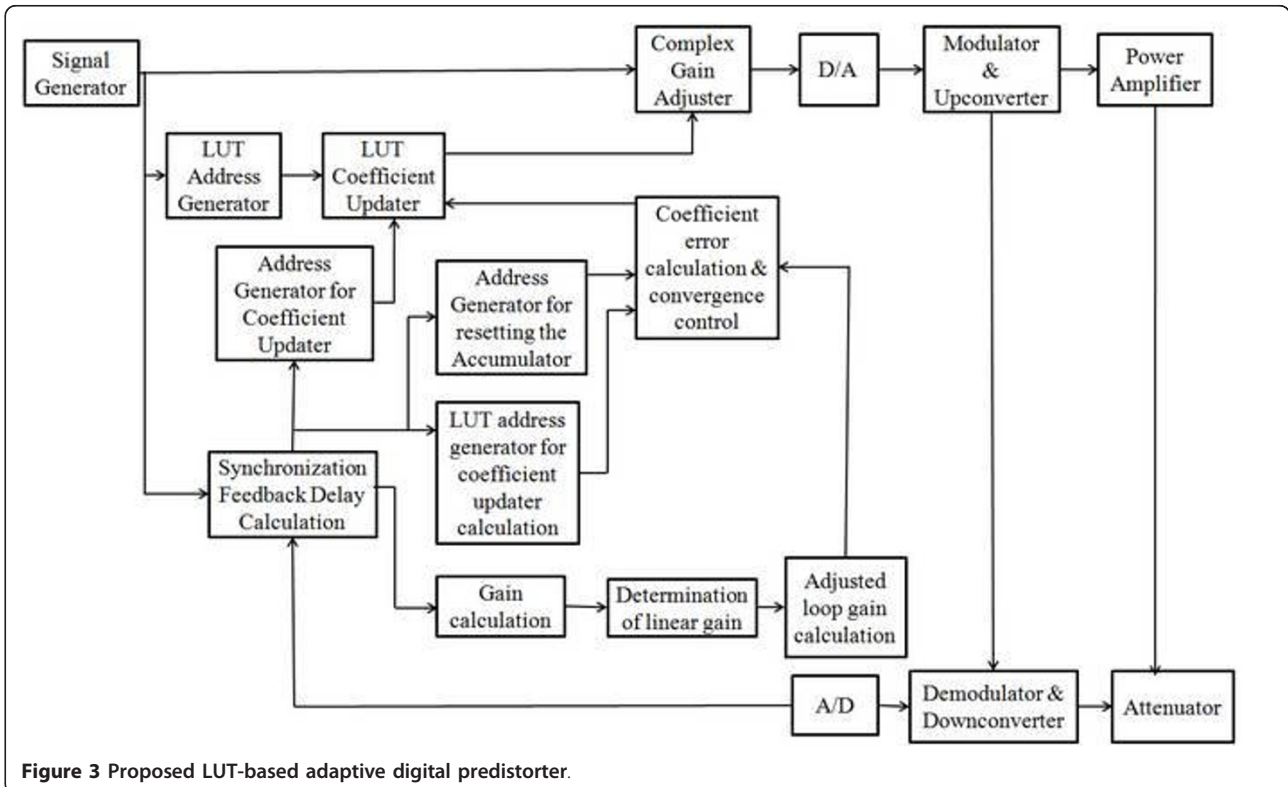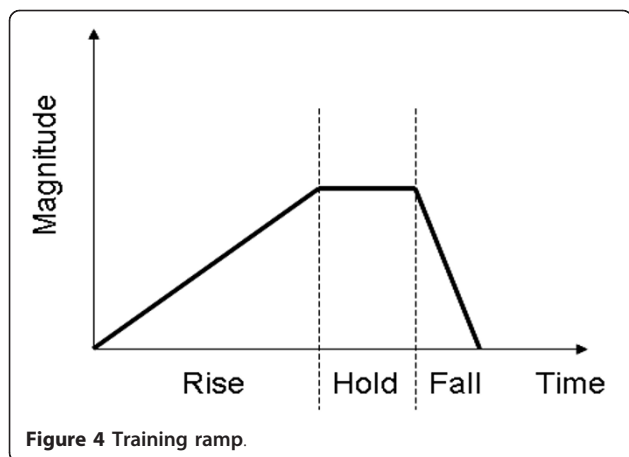

Figure 3 Proposed LUT-based adaptive digital predistorter.

Figure 4 Training ramp.

the LUT address calculation. In the proposed implementation, an optimal spacing scheme for LUT has been used. Optimal spacing has been achieved by applying a suitable compander $C(r)$ to the amplitude signal prior to addressing the LUT. Here, a set of companders C_ρ and C_θ is used that minimizes the total residual nonlinear distortion power at the output of the PA. To simplify the derived mathematical expressions, it is assumed that the input signal's amplitude and the amplifier's gain are normalized to unity. By using a similar approach given in [11], the value of C_ρ and C_θ has been found as

$$C_\rho(r) = \frac{w_\rho(r)^{1/5}}{\int_0^1 w_\rho(r)^{1/5} dr} \qquad (24)$$

And

$$C_\theta(r) = \frac{w_\theta(r)^{1/5}}{\int_0^1 w_\theta(r)^{1/5} dr} \qquad (25)$$

where

$$w_\rho(r) = p(r) \text{ and } w_\rho(r) = | f_\rho(r) h_\theta(r) | \hat{p}(r) \qquad (26)$$

$p(r)$ and $\hat{p}(r)$ are the PDFs of the input amplitude and predistorted amplitude, respectively. Also by using an optimal compander, the total residual distortion power at the PA output remains inversely proportional to N^4 as given in Equations (22) and (23) from simulation results it has been observed that the residual distortion power decreases by 12 dB when the LUT size is doubled as opposed to 6 dB. Thus, combination of linear interpolation with optimal spacing results in higher improvements in PA nonlinearity.
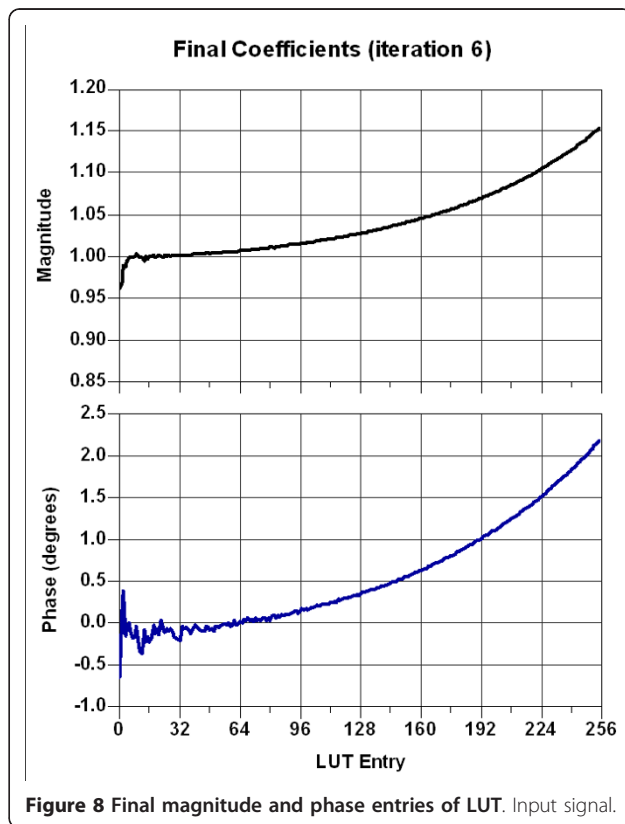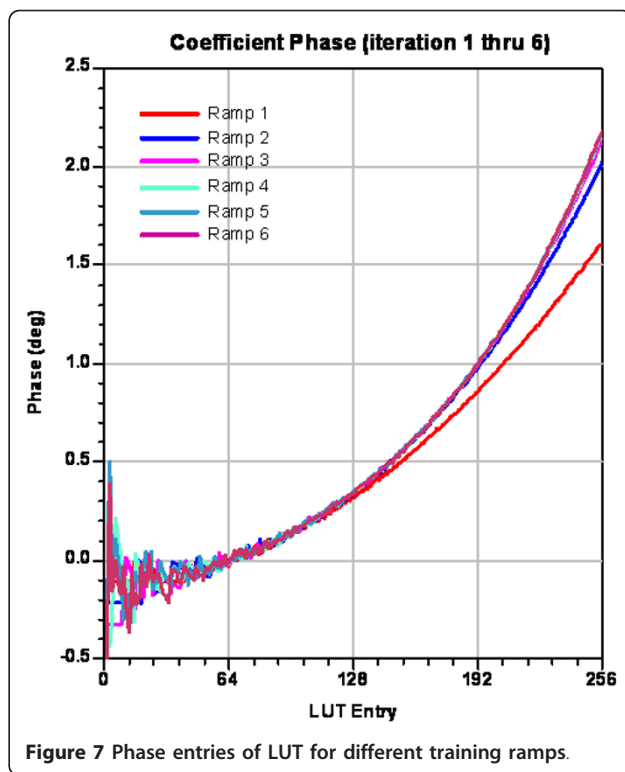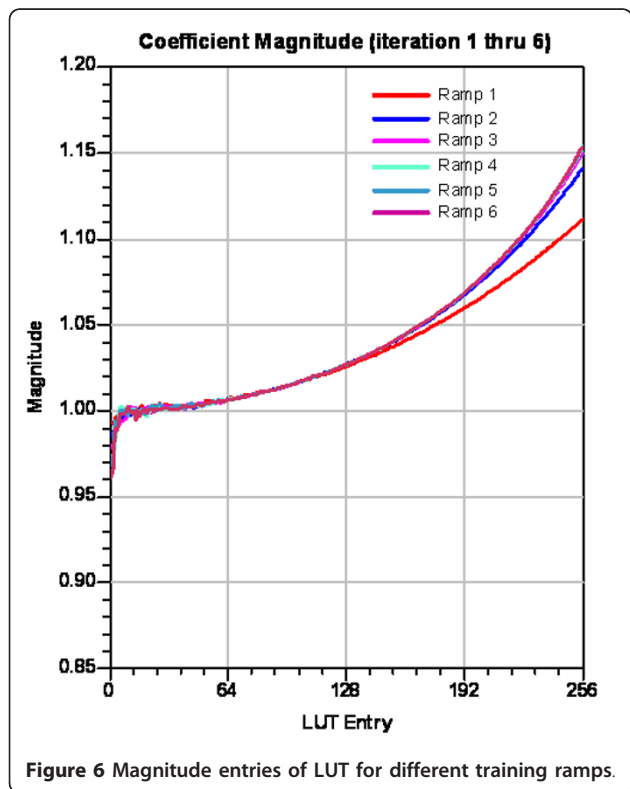
Here, one thing that must be considered is that the compander is implemented as an LUT. It is therefore critical that the additional memory requirements do not offset the gains obtained from using optimal spacing. Thus, the compander has to be implemented as a uniformly spaced, linearly interpolated LUT of size L, forming a piece-wise linear function. From simulation results, it has been observed that as compared to uniform spacing the value of error vector magnitude (EVM) improves by about 10 dB when the LUT size was kept as 256. Also it was observed that as the size of L has been increased beyond 256, no much improvement was found in EVM. Also when both uniform spaced and optimal spaced predistorters were implemented using VHDL synthesis, the gate count has shown almost two times reduction in case of optimally spaced compander.
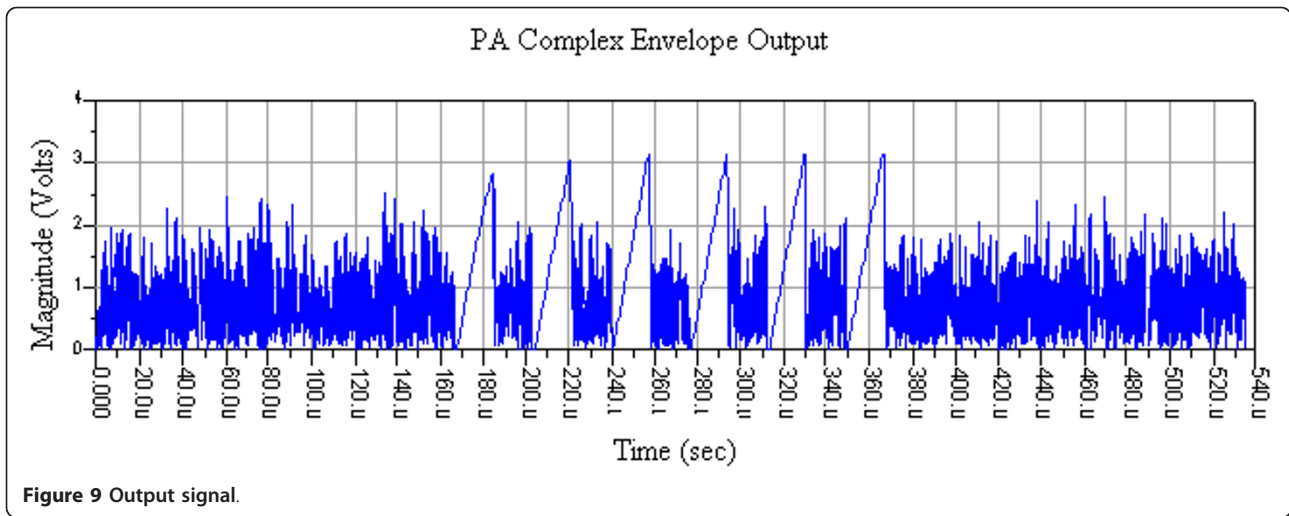
The LUT address generation component translates the magnitude of the baseband input signal into a LUT address using power addressing schemes. The LUT is implemented using the LUT_RAM and the number of entries in the LUT is taken as 256. The LUT is initialized at the outset of the simulation using values read from a pair of text files. The text files have been stored in the data directory, so a path need not be provided

Figure 5 Delay between input signal and feedback signal.
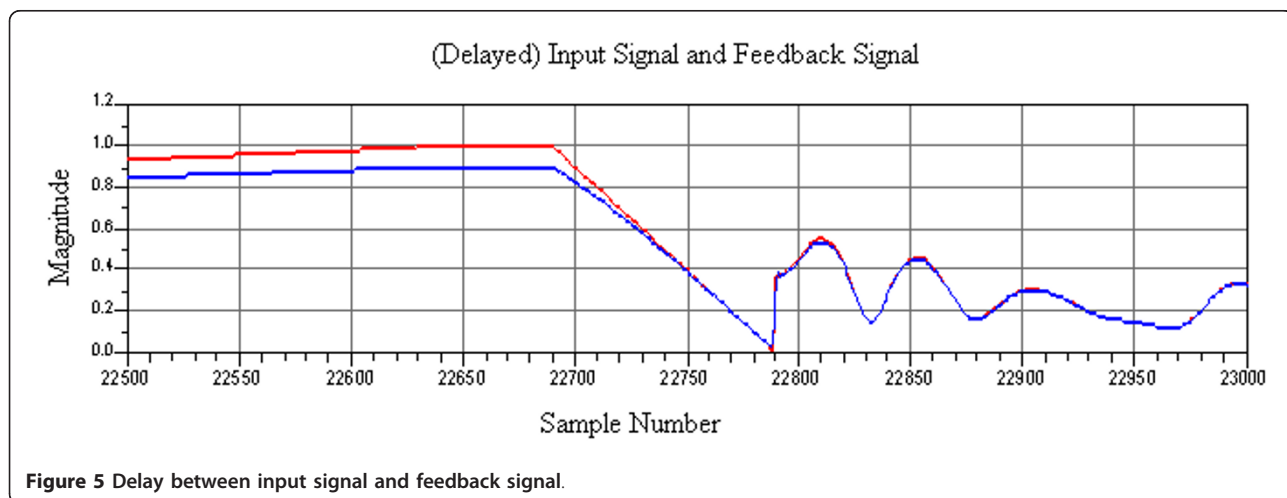
along with the name of the text file. The accuracy of the open loop gain calculation dependents upon the accuracy of the estimation of the delay in the feedback path. The input signal must be delayed precisely by an amount equal to the delay in the feedback path. The delay in the feedback path is estimated by calculating the correlation between the magnitude of the input signal and the magnitude of the feedback signal. The use of the magnitude of the signals has the benefit of not requiring phase synchronization in the feedback path. Because the delay in the feedback path will not necessarily be equal to an integer number of DSP sample periods, interpolation is employed to more precisely align the input and feedback signals. Figure 5 shows the delay calculation between input signal and feedback signal.

The correlation between the input and feedback signal is performed on a modulated signal that precedes the training signal because the gain compression of the amplifier makes the accuracy of the correlation over the training signal suspect. In addition, because the envelope of the modulated signal will typically have a PDF such that it spends much of its time within the linear operating region of the amplifier, correlation using the modulated signal becomes more reliable. However, because the modulated signal is stochastic, the statistics of the modulated signal, as well as the size of the data block over which the correlation operation is performed will

Figure 7 Phase entries of LUT for different training ramps.

Figure 6 Magnitude entries of LUT for different training ramps.

Figure 8 Final magnitude and phase entries of LUT. Input signal.

Figure 9 Output signal.

impact the accuracy of the delay estimation. In general, the accuracy of the estimation improves as the block size increases. Unfortunately, a larger block size requires more memory and takes longer to perform the estimate. The predistortion function cannot be exactly determined following the transmission of single training ramp and recalculation of the LUT coefficients thereafter. A series of training ramps will have to be transmitted. Although significant improvement in the ACPR of the amplifier should be observed even after a single training ramp, yet simulations have shown that the predistortion function can converge to a solution after only six training ramps.

Figure 10 Spectrum of output signal with and without predistortion.
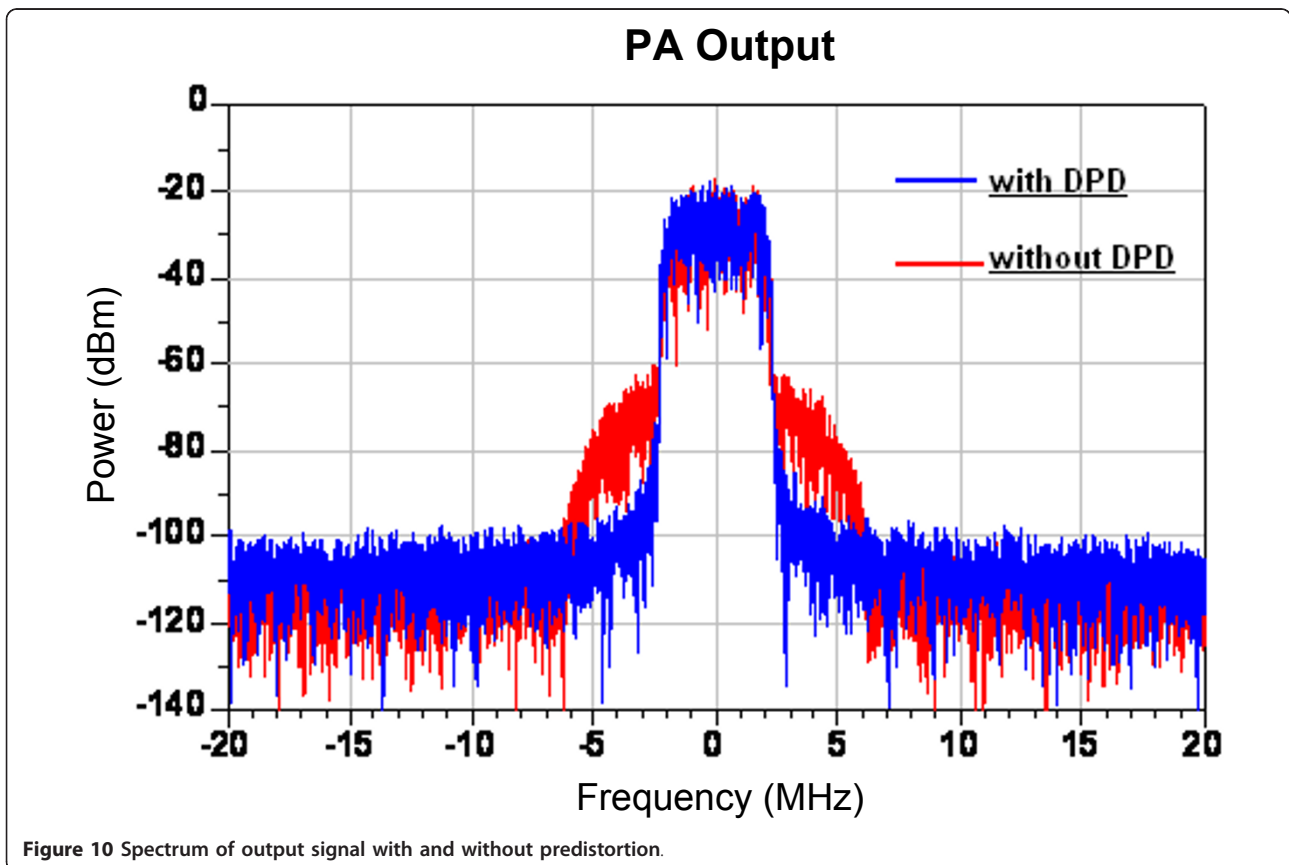
Figures 6 and 7 show the magnitude and phase LUT entries for different training inputs. The final magnitude and phase LUT entries have been shown in Figure 8.

To evaluate the performance of the proposed LUT-based adaptive digital predistorter, the input and output signals of PA have been plotted as shown in Figures 8 and 9, respectively.

The spectrum of the output with and without predistortion is shown in Figure 10. The spectrum shows the capability of the proposed design in suppressing signal re-growth. Calculations show that the proposed LUT-based adaptive digital predistorter reduces EVM to 18.14% and ACLR by 54.19 dB.

4. Conclusions

In this study, a low complexity adaptive digital predistorter with much higher convergence rate as compared to other LUT-based adaptive digital predistorters has been presented. Six training ramps have been used to get high degree of convergence. Although the proposed design shows better performance in terms of reducing EVM and improving ACLR, yet future work will be focused on FPGA implementation of the proposed technique with less hardware requirements.

Competing interests
The authors declare that they have no competing interests.

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