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Improved synchronization, channel estimation, and simplified LDPC decoding for the physical layer of the DVB-T2 receiver

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Abstract

The newly developed 2nd generation standard for digital video broadcasting (DVB-T2) emerges as a significant upgrade over its first generation predecessor DVB-T. The DVB-T2 standard targets an increased system throughput by at least 30% over the DVB-T. This article introduces algorithms in the signal processing chain to improve the mobile operation for DVB-T2. The proposed modified synchronization blocks, along with the improved channel estimation, show significant improvement compared to the results reported in the DVB-T2 implementation guide. In addition, state-of-the-art low-complexity algorithms in the bit processing chain, particularly in the LDPC decoder, are used to provide robustness and support throughput increase, while reducing the implementation complexity. The integrated system is simulated including implementation effects. The simulation results confirm the enhanced performance of the developed integrated model and provide better results compared to those reported in literature.

1. Introduction

The first generation terrestrial digital video broadcasting standard, DVB-T, introduced a breakthrough in TV transmission with well-structured transmission chain that is based on OFDM and powerful forward error correction. Recently, the state-of-the-art technology in the digital communication and the economics of digital transmission has developed considerably, enabling a second generation of the DVB standards to emerge, DVB-T2.

The DVB-T2 standard was introduced in 2010 [1], providing an advancement of the terrestrial video transmission. DVB-T2 can achieve a capacity increase by at least 30%. compared to its predecessor DVB-T [2]. In fact, DVB-T2 is taking serious steps to effectively replace the DVB-T in Europe. Several innovative business models to benefit from its improved capacity and performance have been developed [3]. However, the ambitious increase in the throughput can be useful under mobile channel conditions only if the DVB-T2 receiver is carefully designed. More specifically, the channel estimation and

synchronization blocks play the main role in enhancing the performance in mobile reception scenarios.

This article focuses on improving the performance of channel estimation and synchronization blocks along with a low-complexity LDPC decoder. A modification to the synchronization block is added to improve its performance and eliminate the need for an extra timing synchronization stage. Efficient implementation, with improved performance channel estimation, is employed to better suit the mobile channel compared to the rather limited channel estimation proposed in the DVB-T2 implementation guide [4]. On the other hand, a low-complexity layered decoder is employed to reduce the implementation cost of the LDPC decoder. By combining these modifications together, an enhanced performance lower complexity DVB-T2 receiver is obtained. Numerical results show improved performance of the integrated design when compared to results reported in an example existing industrial solution [5] as well as improved performance of the individual targeted blocks when compared to the implementation guide [4].

The remainder of the article is organized as follows: Section 2 is dedicated to the improvement in the receiver signal processing chain, namely, the introduced

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algorithms for synchronization and channel estimation. Section 3 highlights the LDPC decoder employed in the receiver along with possible efficient storage procedure of the parity check matrix which helps in reducing the complexity and memory requirement. Section 4 introduces the integrated DVB-T2 model simulation results in different channel conditions. Section 5 presents a conclusion and summary of the study.

2. Improved DVB-T2 synchronization and channel estimation design

The general structure of the DVB-T2 receiver signal processing chain is shown in Figure 1. The signal processing chain in the receiver is mainly responsible for compensating the channel effects and performing synchronization and proper detection of the frames. This section presents our contribution towards modifying critical blocks in the signal processing chain, namely the synchronization block [including frame synchronization, i.e., coarse time synchronization and coarse frequency offset (CFO) compensation], and the channel estimation block. The algorithms used in the design of these blocks are either newly developed or improved implementations of selected state-of-the-art algorithms in wireless communications. They meet the requirement of robust and improved performance while maintaining low-complexity constraints.

2.1. Synchronization

Accurate synchronization should be implemented to achieve robust reception of the DVB-T2 signal. In general, the synchronization process in DVB-T2 is achieved in two categories:

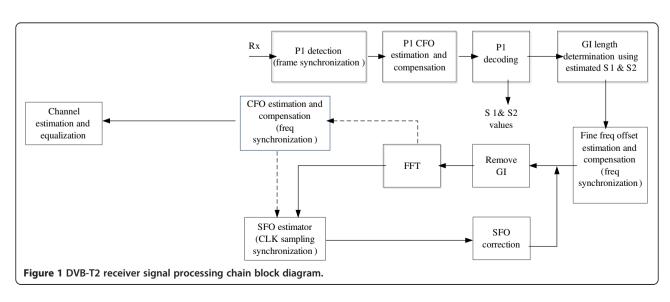
 (i) Timing synchronization: Coarse time synchronization (Frame synchronization), and fine timing synchronization. (ii) Frequency synchronization: Both fine and CFO estimation and compensation.

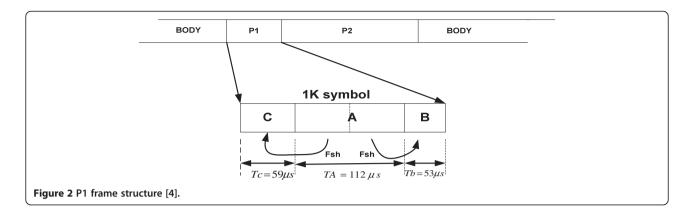
2.1.1. Coarse time synchronization

In this section, we propose a modification to the coarse time synchronization block to improve its performance. This is done in two steps: (1) Changing the correlation circuit involved in the detection of preamble P1. (2) Threshold comparison circuit with emphasis on choosing an appropriate threshold level.

The T2-frame always begins with a P1-preamble that has a special structure as shown in Figure 2. The first stage in synchronization, referred to as "Frame synchronization", intends to capture the start of the T2 frame. DVB-T2 makes major use of the special structure of the preamble P1 in achieving synchronization. The main middle part of the P1 symbol, called part A, comprises an OFDM symbol which has a length $N_{\rm A}$ of 1024 subcarriers. This part of the P1symbol is surrounded by two frequency shifted versions of the part A. The part C in the P1 symbol is of length N_c = 542 and it is a frequency shifted version of the first 542 samples of middle part A. The part B of length $N_{\rm B}$ = 482 is a frequency shifted version of the last 482 samples of part A. The DVB-T2 implementation guide presents an algorithm for coarse timing synchronization using P1. This algorithm is based on a double branch correlator.

In our proposed circuit, the original algorithm provided in the implementation guide is further modified into two ways. In order to achieve an accurate estimation of the FFT window position (in case of no fading), the running average filter span is modified to the length $T_c = N_c \times T$ in the upper branch and the length $T_B = N_B \times T$, in the lower branch instead of T_A , where $T_A = N_A \times T$, and T is the chip rate. The modified correlation circuit is shown in Figure 3. In the figure, the delay applied in



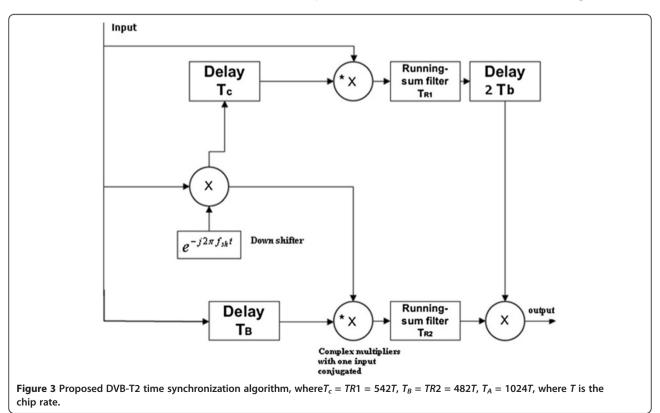


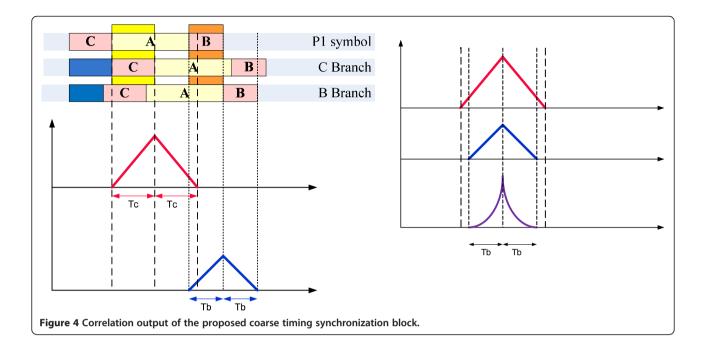
the upper correlation branch is also modified to $2T_B$ instead of the original length T_A . These modifications not only improve the resulting peak of the correlation, but also reduce the computations required in the synchronization operation. Figure 4 presents the output of the correlation of the proposed P1 detection circuit. The figure indicates that the proposed design eliminates the flat trapezoidal shape which results in the original algorithm correlation output, and produces a clear peak indicating a clear maximum of the correlation with quadratic decaying neighboring points. Thus, the need for an extra fine timing symbol synchronization step is eliminated.

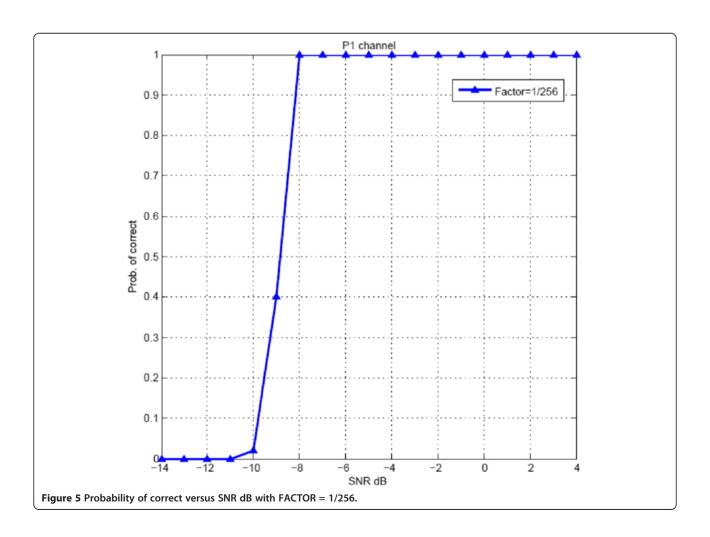
The threshold comparison block is our second modification to enhance the peak detection. The resulting correlated signal output is compared to a threshold related to the power in the P1 signal. In the previous algorithm, a suitable threshold could be calculated as follows:

$$Threshold = FACTOR \times E_B \times E_c \tag{1}$$

where E_B is the energy in the samples with length T_b preceding the peak position in branch B, E_C is the energy in the samples with length T_c preceding the peak position in branch C, and FACTOR is decided through the simulations. Figure 5 shows the probability of correct detection for FACTOR = 1/256 which is better than the resultant one shown in the DVB-T2 implementation







guide [4] in case of AWGN channel. The peak is not declared directly after exceeding the threshold. However, when this threshold is exceeded by the correlation output, the correlation values after the threshold are kept for a predetermined period to choose the maximum value. This limits the possibility of false detection of P1, when the frame is not captured at its beginning. It is worth noting that in [6], similar work was delivered independently based on modifying the implementation guideline circuit. This modification is used to produce a modified P1 detection circuit with linear decaying rate around the maximum peak.

The algorithm is tested under Rayleigh Channel fading (Mobile Channel, TU-6) which has been defined by COST 207 [7] as a typical urban profile. TU-6 is mainly composed of six paths having wide dispersion in delay and relatively strong power. Figure 6 shows the histogram of the peak detection position. Using our modified algorithm enhances the performance of this coarse timing estimation step. The modified synchronization algorithm needs only a maximum margin of 16 points into the guard interval to insure the position in the cyclic prefix.

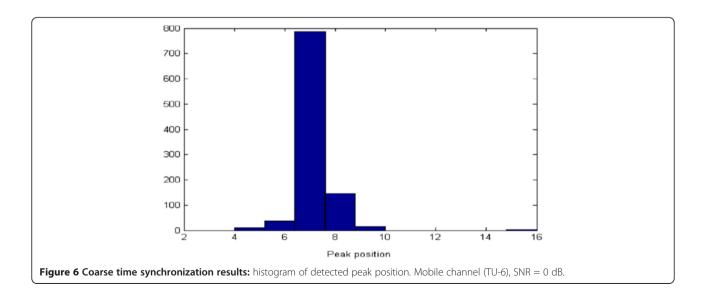
2.1.2. CFO

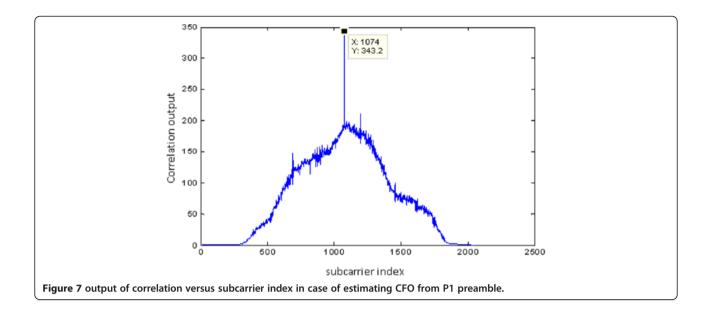
The fractional part of the frequency offset is estimated and compensated using the algorithm in the DVB-T2 implementation guide [4]. The integral part of frequency offset is referred to as CFO. CFO can be estimated in two stages using P1 and P2 symbols in the frequency domain. The DVB-T2 implementation guide does not disclose a specific detailed procedure to estimate and compensate the CFO. In the following we present our proposed modified CFO estimation and compensation, which is based on a modification of the algorithm in [8]

to improve its performance when applied to the DVB-T2 signal.

CFO is done in two stages. In the first stage, FFT of resolution 1024 is applied to the detected time domain P1 symbol (the main part of the P1 symbol, i.e., part A) then a correlation is done between the active carriers and the detected P1. This operation is repeated for shifted versions of active carriers. The initial estimate of the coarse offset is compensated for in the rest of the frame by multiplying with the inverse phase. Simulation of the modified CFO is done under the assumption of SNR = 0 dB, Rayleigh fading and offset equals to 50 subcarrier spacing of 1024 OFDM signal. The result is shown in Figure 7. In the second stage, the residual CFO is estimated using the continual pilots P2 symbol similar to the algorithm in [8].

The algorithm for the second stage of the CFO recovery is modified by comparing only a specific subset of the P2 pilots recorded in lookup tables. The modification is required because of the intricacies of DVB-T2 signal in case the CFO is equal to, or more than, three times subcarrier spacing in the presence of Rayleigh channel and with strong noise. This will generate more than one peak leading to an erroneous decision. This is due to the nature of the pilots, which repeat every three subcarriers. For example, if the CFO = 3 times subcarrier spacing, then we shift the received signal for correlation process from -15:15 and at shift = 3. There are several pilots which can, in the presence of channel and noise, produce a second peak with a wrong decision as illustrated in Figure 8. This problem is eliminated using the new proposed algorithm as shown in Figure 9. Thus, the pilots that cause the problem are eliminated and the appropriate subset of pilots is stored in lookup tables. Figure 10 illustrates the probability of correcting the

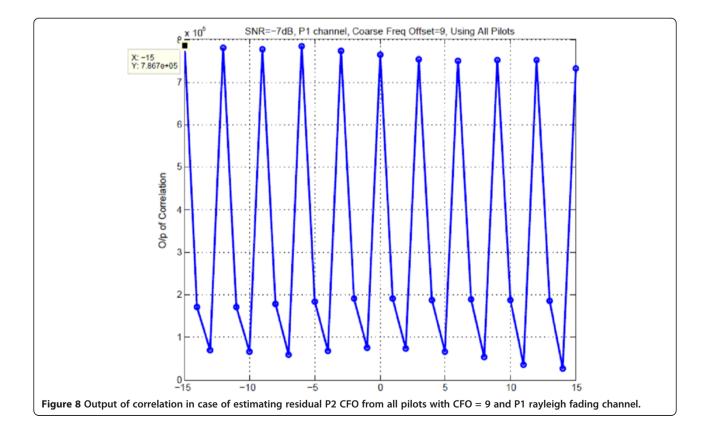


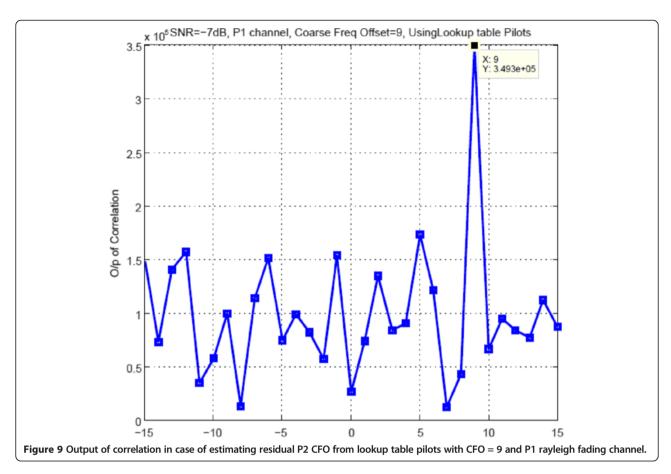


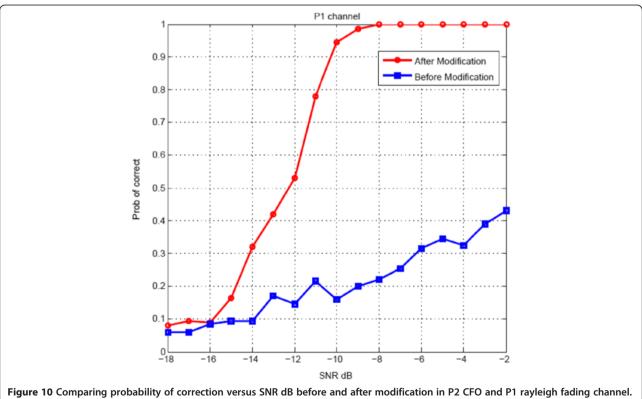
residual CFO estimation from P2 before and after modification. The algorithm, based on comparing the pilots to a lookup table, was implemented according to the flowchart in Figure 11. The construction of the lookup table is done based on two sets of pilots extracted either from two consecutive P2 symbols for FFT sizes ranging between 1-k up to 8-k or only one symbol in case of

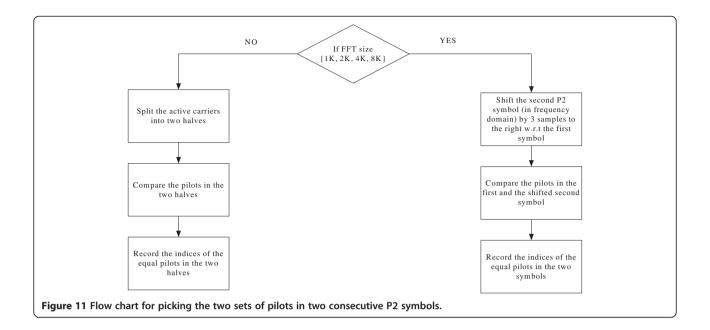
FFT sizes 16K or 32K (in this case, they are split into two halves). A record of similar pilots' indices in the two sets is formed by comparing the two pilot sets in the first symbol and the shifted second symbol for all the FFT sizes and using it as lookup table.

Using the lookup tables, the CFO is estimated as illustrated in Figure 12. The algorithm is applied and









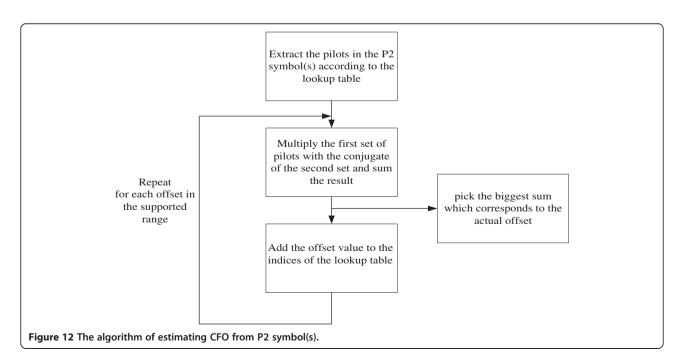
repeated with different positive and negative offsets, and then the peak is picked corresponding to the CFO.

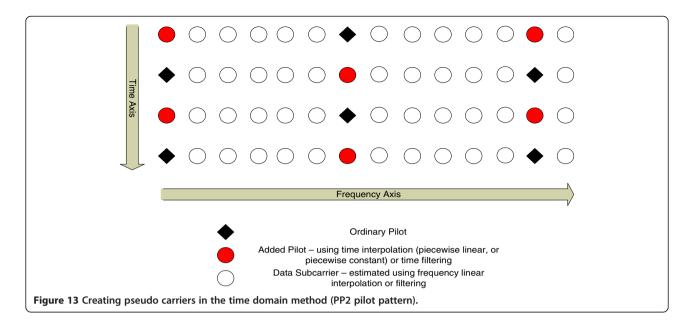
2.2. Channel estimation

The channel estimation suggested by the DVB-T2 implementation guide is a linear interpolation channel estimator in both time and frequency directions, which has the advantage of low complexity but its performance is very poor in fading channels. Instead we employ a robust estimator that does not require the channel profile knowledge. Although its implementation complexity is comparable to

the linear channel estimator, the performance of the robust estimator is, by far, superior to the linear estimator currently reported in the DVB-T2 implementation guide.

In general, DVB-T2 operation in fading channels is directly affected by the channel estimation technique used. The choice of the channel estimation becomes more crucial with the DVB-T2 migrating to mobile application. A careful inspection of the channel estimation utilized in the DVB-T2 implementation guide reveals its reliance on 1D cascaded linear interpolation in time and frequency domains. However, the performance of this





first-order interpolation is generally mediocre [9]. The literature of channel estimation classifies the estimator types into two main categories: Decision directed and pilot-aided channel estimation (PACE). The DVB-T2 provides eight different pilot patterns, named PP1,..., PP8, which implies clearly limiting our search to the pool of the PACE algorithms which generally perform better than the decision directed algorithms. In the literature of PACE algorithms, minimum mean square error (MMSE), also referred to as Wiener-based estimator, stands out as the measuring stone to all other algorithms. MMSE provides the optimal linear estimation in the mean square error (MSE) sense [10,11]. However, a major problem with MMSE estimation is that it requires the knowledge of the exact channel correlation functions. The channel correlation functions are usually unknown and time varying, which makes this technique impractical. This is one of the main reasons the DVB-T2 implementation guide favored linear interpolation. In fact, the linear interpolation method is chosen mainly due to two main factors: the first is its simplicity; the second reason is its independence of the changing channel profile in mobile environment.

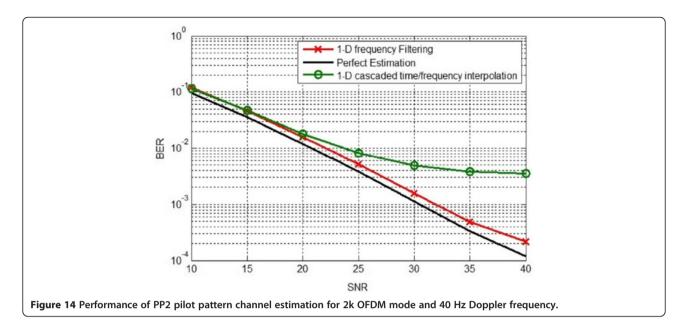
In [10], a robust MMSE channel estimation is developed. The robust algorithm is based on using a generic robust correlation function that gives acceptable MSE for all channel correlations. The used solution employs a uniform power delay profile which is longer than the channel delay spread as well as a uniform Doppler spectrum profile with Doppler frequency higher than that of the channel. The main advantage of this algorithm is that the filter coefficients do not depend on the channel profile. They can be calculated *a priori* and stored in a memory at the receiver side to be applied on the least

squared (LS) estimate of the channel at pilot positions. The robust estimator has many advantages: (1) It exhibits performance which is very similar to the optimal channel estimation. (2) It does not require the knowledge of the channel profile and is thus immune to degradation in performance when operating in a fast changing mobile environment. (3) The complexity of the robust estimator is much less than the MMSE solution. The robust estimator depends on a single channel profile and the filter coefficients are pre-computed and stored. This relieves the load of an on-line updated calculation of the channel coefficients which includes the inversion of a high order matrix.

A one-dimensional (1D) cascaded linear interpolation/Robust Wiener filtering is considered for the channel estimation. During the first step, anLS estimate of the channel response is made at the pilots, then linear interpolation is carried out in the time domain to obtain accurate estimations at the in-between subcarriers. Linear time interpolation or "time averaging" is used to get the pseudo pilots that are the circled subcarriers illustrated in Figure 13. In the second step, frequency domain estimation utilizes both the original pilots and

Table 1 The simulation configuration for channel estimation

Parameter	Specification
FFT size	2048
Number of available carriers	1705
Signal constellation	16 QAM
Guard interval	1/8
Scattered pilot pattern	PP2
Channel model	TU6

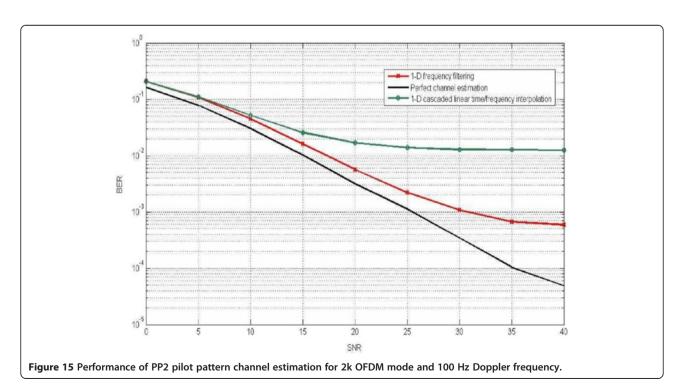


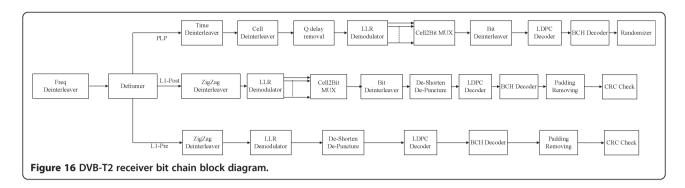
the newly generated pseudo pilots. The pilots are passed to the 1D filter (1D robust MMSE) to get the remaining data subcarriers in each symbol:

$$\widetilde{H}[m] = \sum_{m_1 \in p_m} C[m_1] \widetilde{H}[m_1], \qquad (2)$$

Where $\widetilde{H}[m]$ is the estimated complex channel frequency response at location m on the time/frequency grid, and $\widehat{H}[m]$ is the LS estimates for pilot locations and the time interpolated pseudo-pilots. $C[m_1]$ is the

complex Wiener filter coefficients that can be calculated as in [12], and m_1 belongs to the indices of the nearest LS pilots in the same OFDM symbol to the required subcarrier m. The set P_m represents the N_t pilot locations near m where N_t is the number of the filter coefficient. When utilizing the nearest pilots in the frequency domain estimation, the middle part of the coefficients is periodic. Using this property the calculation process of the robust filter coefficients can be further reduced by up to 90% in some cases. This could be valuable, with





the need to store the coefficients for the different pilot patterns and different OFDM sizes.

The method, referred to as "1D frequency filtering", is compared to the method proposed in the DVB-T2 implementation guideline, referred to as "1D cascaded time/frequency interpolation". In our simulation, perfect time and frequency synchronization is assumed. The simulation is applied to TU6 channel model with Doppler shifts of 40 and 100 Hz. The chosen bandwidth is 8 MHz. Table 1 presents the simulation configuration parameters.

Figures 14 and 15 present the bit error rate (BER) performance of PP2 scattered pilot pattern for Doppler frequencies 40 and 100 Hz, respectively. The figures clearly show the improved performance of the robust estimator. This improvement comes at minimum possible added complexity as the robust algorithm utilizes hybrid linear time interpolation/robust frequency interpolation. Recently, the research group came across a linear minimum square errorproposed for DVB-T2 system in [13]. The channel estimation in [13] is simulated using the same channel parameters we used in Table 1, except for using QPSK mapping rather than the 16 QAM constellation which we employed. The QPSK is known to have a better error rate performance. However, even with the higher 16 QAM constellation we used, the 1D frequency filtering channel estimation employed here outperforms the reported results in [13] for the respective scattered pilot patterns. Similar results were obtained for different pilot patterns and different OFDM sizes.

3. Bit processing chain

The improved structure of the signal processing chain of the DVB-T2 receiver is complemented with an enhanced bit processing chain structure to improve the overall performance of the receiver. The bit processing chain structure is illustrated in Figure 16. The implementation of the bit chain receiver involves a state-of-the-art log-likelihood soft demapper, and BCH decoding [14-16]. On the other hand, the LDPC decoder poses a particular implementation challenge regarding the algorithmic and implementation complexity, not to mention its memory requirements. To begin with, an efficient low complexity-

high performance decoder is required. To reduce the memory requirements, an efficient storage procedure for the parity check matrix at the receiver side is also needed.

3.1. Layered decoding for DVB-T2 LDPC codes

LDPC codes are first introduced as linear binary codes [17,18]. The Tanner graph [19] is used to represent connections and edge links. An edge links the check node i to the variable node j if the element H_{ij} of the parity check matrix is non-null. Decoding algorithms based on Tanner graphs are iterative, based on exchanging information between parity check nodes and variable nodes. Belief propagation is applied to Tanner graphs to efficiently decode LDPC codes [20,21].

Soft decoding algorithms dominate the scene in real application of LDPC decoding. In general, LDPC decoding algorithms can be seen as an approximation of belief propagation decoding. Improvements to the belief propagation through scaling have been addressed in several publications [21-24]. Min-Sum decoding is used in our proposed decoder. The main reason for this choice is its relative implementation simplicity and its robustness to quantization errors when implemented on hardware. A modified normalized Min-Sum update is used to speed the convergence of the Min-Sum algorithm [22]. The detailed complexity comparison of the different LDPC codes and their quantized performance is detailed in [22,23].

To make the encoding and decoding of LDPC codes in DVB-T2 more efficient, the sparse part of the parity

Table 2 Normal frame parameters for layered LDPC decoder

K _{LDPC}	N _{LDPC}	$R = R_{code}$	Q_{LDPC}		
32400	64800	1/2	90		
38880	64800	3/5	72		
43200	64800	2/3	60		
48600	64800	3/4	45		
51840	64800	4/5	36		
54000	64800	5/6	30		

Table 3 Short frame parameters for layered LDPC decoder

	A/			
K _{LDPC}	N _{LDPC}	R _{code}	R	Q_{LDPC}
3240	16200	1/4	1/5	36
7200	16200	1/2	4/9	25
9720	16200	3/5	3/5	18
10800	16200	2/3	2/3	15
11880	16200	3/4	11/15	12
12600	16200	4/5	7/9	10
13320	16200	5/6	37/45	8
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check matrix is designed to be in a quasi-cyclic form [25,26]. Thus, further efficient manipulation of the structure of the parity check matrix can make it suitable for layered decoding [27-29].

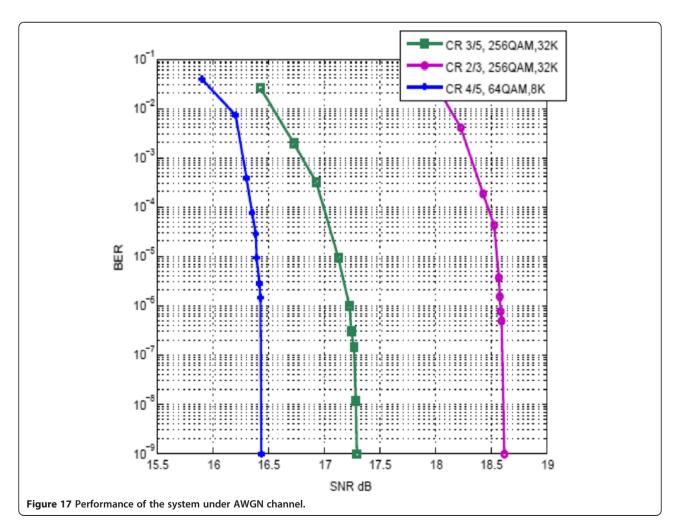
The employed decoder makes use of the concept of layered decoding [28,30,31]. Layered decoding approaches the parity check matrix as a sequence of elementary matrices or layers. The soft-decoding algorithm is then modified to work on these layers. The regular iteration done on the whole parity check nodes is divided into $Q_{\rm LDPC}$ separate sub-iteration, where $Q_{\rm LDPC}$ is the number of layers in the parity check matrix H. In our implementation, the layer size is 360. The different values for $Q_{\rm LDPC}$ are given in Tables 2 and 3.

In each sub-iteration, the soft bits are updated and the syndrome is calculated and checked. If the syndrome is zero, a valid codeword is obtained and the decoder concludes the decoding. Otherwise, the decoder proceeds to the next sub-iteration with updated version of soft bits and the process continues until it reaches the maximum number of iterations.

The breakup of the iteration into sub-iterations improves the convergence speed. The number of iterations required for layered decoding is generally half the number of iterations needed for the regular LDPC decoder [27,28,32].

3.2. Storage method of the parity check matrix

The quasi-cyclic structure of the sparse part of the parity check matrix can be better exploited to serve the layered structure of the decoding algorithm. In the following, we



present one possible way of storing and regenerating the H matrix that is capable of producing the submatrices in each layer separately, without the need to reproduce the whole matrix H at once. Consider the information part, which can be viewed in each layer as $Z_{\rm LDPC}P$ matrices where P is a 360 × 360 matrix and $Z_{\rm LDPC} = K_{\rm LDPC}/360$. These matrices may be zero, identity, shifted version of identity matrix, or (2, 3, and 4) different shifted versions of identity matrix added together. The maximum number of possible shifts is 360 and the maximum number of additions corresponds to the maximum number of 1's in a column, i.e., equals to 4.

As the 1's positions in the shifted P matrices are non-overlapping, the addition of the four matrices corresponds to the different shifts. This property can be exploited through substituting with a "for" loop to sequentially regenerate the 1s in the P matrix at hand. The following pseudo code illustrates the general idea of how to reproduce a P matrix in the information part within a certain layer.

```
Initialize: Matrix at position U_{\rm LDPC} = 0_{360\times360}; If P_{\rm shift}(1:4) > 360

Exit; Else

For i=1:4

For C=1:360

C_u=360\times(U_{\rm LDPC}-1)+C

R_u=(P_{\rm shift}(i)+C) mod 360

End

End

End
```

where $U_{\rm LDPC}$ represents the order of matrix in layer, $U_{\rm LDPC}=1,2,3...,Z_{\rm LDPC},$ C represents the column index inside the P matrix, C=1,...,360, C_u represents column index in the matrix at position $U_{\rm LDPC}$ in the layer, R_u represents row index in the matrix at position $U_{\rm LDPC}$ in the layer.

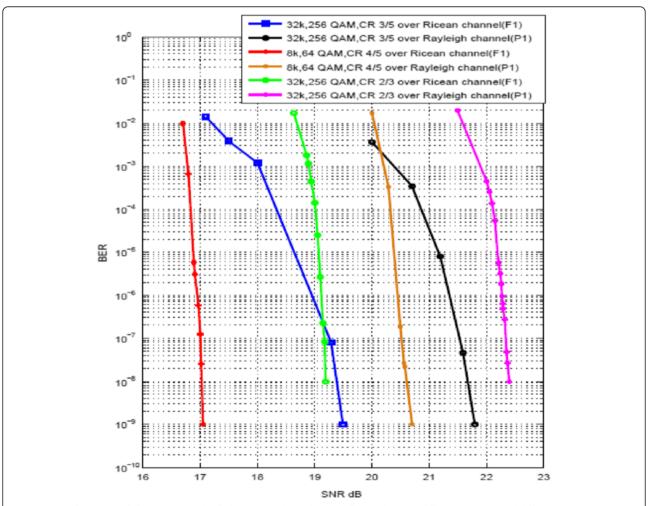


Figure 18 Performance of the system under fading channel condition. Different channels, different FFT sizes and different code rates in case of PP2 scattered pilot pattern.

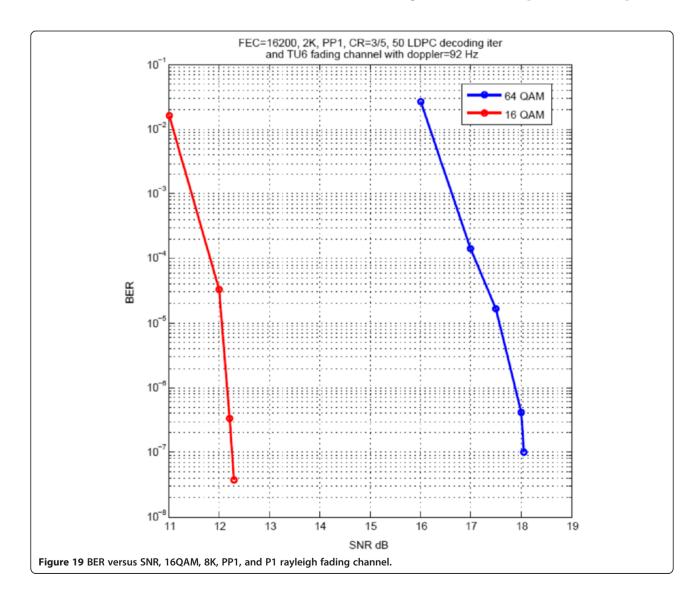
The information part of H matrix can be stored in $Q_{\mathrm{LDPC}} \times Z_{\mathrm{LDPC}} \times 4 \times 9$ bits. The 9 bits represent the four possible shifts $P_{\mathrm{shift},t} = 0,\ldots,359, i = 1,\ldots,4$. Any number in the $P_{\mathrm{shift},t}$ larger than 359 indicates that the P matrix is all zeros. Q_{LDPC} and Z_{LDPC} are system parameters which are dependent on code rate and frame type (short or normal frame). This storage method operates on the parity matrix to represent it in the closest form to quasi-cyclic submatrices. It is capable of producing the layers separately, and thus suits the operation of the layered decoding that doesnot require all the nodes of the H matrix, but rather the intended layer the decoder operate on. Using the concept of layered decoding can reduce the memory requirements and logic operation by up to 50% [33].

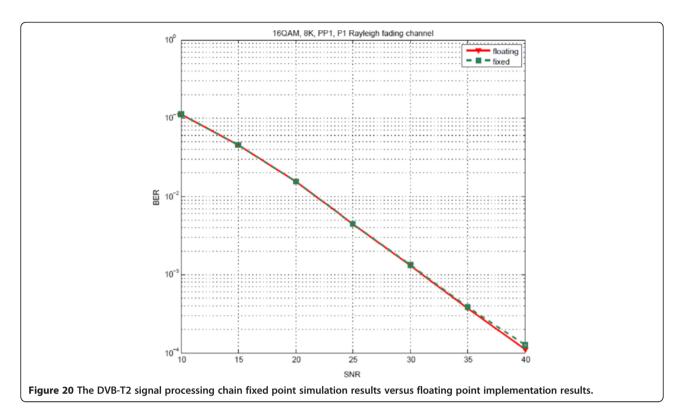
4. Simulation results

The integrated DVB-T2 receiver is simulated under different channel conditions and various channel models.

Few publications address the complete DVB-T2 receiver simulation. The integrated simulation results in case of AWGN channels are shown in Figure 17. Compared to the result reported for AWGN channel in [5], our integrated results provide better performance in all the tested FFT sizes, rates, and QAM constellations. In particular in case of 32K, 256 QAM, CR = 2/3, the proposed integrated DVB-T2 receiver is better than the corresponding curve in [5] by around 0.6 dB.

Figure 18 presents the simulation results of our integrated receiver for Rayleigh fading channel (P1) and Ricean fading (F1), defined according to the DVB-T2 implementation guide [4]. Other integrated DVB-T2 results are presented in literature as in [34]. The proposed integrated DVB-T2 receiver results show consistent improved performance to the results reported in [34]. The difference in performance varies according to the simulation parameters. Compared to





the results reported in the DVB-T2 implementation guide, our integrated DVB-T2 receiver performs comparably. It is worth noting that the DVB-T2 implementation guide assumes perfect channel estimation and synchronization. Nevertheless, the performance loss of the proposed integrated DVB-T2 receiver compared to perfect signal processing chain operation is relatively small and indicates a very good performance of the different channel estimation and synchronization blocks proposed. Figure 19 shows the performance in case of TU6 fading channel with Doppler = 92 Hz for 64QAM and 16QAM and CR = 3/5. Figure 20 illustrates that there is very little loss between floating and fixed point models in signal processing chain.

5. Conclusion

This article presents modifications to key blocks in the DVB-T2 receiver. Throughout our design of the DVB-T2 receiver physical layer we targeted real-life operation scenario of DVB-T2, taking into consideration the mobile channel. Several new ideas, along with utilizing state-of-the-art algorithms have been developed with two main targets in mind. The first is to provide improved performance suitable for mobile channel conditions and the second is to preserve the low implementation complexity mandated by the nature of a mobile device. The modifications proposed are concerned with the synchronization, channel estimation, and forward error correction decoding of DVB-T2 receiver. In the

synchronization block, a modified coarse timing synchronization is presented that solves the problem of the trapezoidal shaped autocorrelation circuit presented in the implementation guide. The CFO is also modified by adding an additional stage to improve the accuracy of the coarse offset estimator. The concept of operation of the modified CFO is carefully selected from the literature. However, it is modified to suit the special nature of pilots used in the DVB-T2. In the channel estimation block, we emphasize and focus the attention on one carefully selected robust channel estimator. The proposed estimator outperforms the legacy zero forcing channel estimator without adding the complexity burden of the optimal MMSE estimator. The layered decoding concept is used in the LDPC along with one possible storage method that rearranges the H matrix to better exploits quasi-cyclic structure. The DVB-T2 receiver results were presented for the integrated performance after applying the modifications. The integrated DVB-T2 system is tested for different code rates and under various channel models. The simulation results prove the improved performance of the proposed DVB-T2 receiver.

Competing interests

The authors declare that they have no competing interests.

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