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RF low power subsampling architecture for wireless communication applications

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Abstract

With the increasing demands of wireless communication, flexible, complex, and diversified wireless communication applications are required. However, the difficulty of enabling new wireless communication applications is the lack of low power radio frequency (RF) transmission devices, especially the RF receiver. In order to alleviate this problem, an RF low power subsampling architecture for wireless communication applications is proposed in this paper. This subsampling architecture adopts a single-ended to differential configured balun low noise amplifier (balun-LNA), a subsampling mixer with high sampling ratio and a finite input response (FIR) filter and infinite impulse response (IIR) filter achieving frequency down-conversion, avoiding using high power-hungry blocks. Based on a subsampling theory, an optimum sampling frequency for the subsampling architecture is necessary to relax the complexity of the system. For the application of internet of things (IoT) wireless communication, the paper provides the implementation of the subsampling receiver solutions to get a tradeoff between power consumption, gain, noise, and sensitivity. It can achieve −85 dBm sensitivity for an amplitude shift keying (ASK) modulation at the data rate of 1 Mbps with the clock sampling frequency of 40 MHz. Finally, the theoretical analysis and simulation results show that the performance of the subsampling architecture has several advantages over others.

Keywords: RF subsampling receiver, balun-LNA, 780 MHz IoT, Low power

1 Introduction

Thanks to the evolvement of the CMOS technology, the RF integrated circuits can improve integration and reduce chip area greatly. With the improving demands for wireless communication and the emerging new technologies in recent few years, there is growing attention on sub 1 GHz Industrial, Scientific, and Medical (ISM) bands [1]. Different regulations are applied in different countries, for example, in the USA, the band from 902 to 928 MHz is adopted, with central frequency 915 MHz, while in Europe and China, the bands from 863 to 868 MHz and 755 to 787 MHz are applied, respectively [1, 2]. Most of these standards focus on high integration, low power, low cost, and multi-mode [3]. Especially, low power and high flexibility are of great importance [4, 5].

Although some low power architectures of receiver have been reported, such as direct conversion architecture and low intermediate frequency (IF) architecture [6–8], highly power-hungry blocks such as LO and RF PLL are still existing in the circuits. Fortunately, the concept of new sampling technique is introduced in [9], called software-defined radio (SDR), which can directly digitize and demodulate all signal from the antenna by A/D converter (ADC). Although this sampling technique can massively reduce power consumption of the system without using RF/analog blocks, it increases the memory of ADC which cannot be achieved by using the existing technologies. Moreover, a specific architecture of new RF sampling approaches can directly down-convert RF signals to baseband signals and achieve signal processing and demodulation in the digital circuits, which can minimize the number of RF and analog blocks [10–12]. For example, RF front-end mainly includes a low noise amplifier and a mixer, which achieves subsampling frequency conversion with clock down-sampling with embedded filtering [12]. However, the fixed filters restrict flexibility of the receiver, which cannot be suited for more channel transmission.

Meanwhile, regardless of RF PLL, subsampling receivers have great advantages in terms of power consumption and

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flexibility by adopting low sampling frequency [13, 14]. For example, the multi-channel receiver with channel filtering at RF has been reported in [14], which can achieve −78 dBm sensitivity at 10^{-3} BER for BFSK modulation. However, the architecture based on the BAW resonator has been implemented, which cannot be integrated for the system. In order to improve integration of the subsampling receiver, the number of extra exponents should be minimized. An active balun-LNA with the noise-cancelling technique instead of off-chip balun can be used [15–17]. For example, the active balun-LNA for GPS can exhibit a power consumption of 3.6 mW and a noise figure of 1.8 dB [17]. Moreover, low supply voltage can make power consumption further reduced [18, 19], with the 0.5 V supply voltage, the total power consumption of the receiver is about 1.15 mW [19]. However, low supply voltage can lead to the nonlinear effects and increase the noise figure of the system [20]. In addition, a quadrature down-conversion technique can greatly improve efficiency of signal frequency conversion, such as subsampling receiver with Q-enhanced RF filtering exhibiting −87 dBm sensitivity at 10^{-3} BER [21].

In this paper, design of the subsampling architecture should be tradeoff between integration, sensitivity, noise figure, and power consumption for the application of IoT. In order to solve the problem of noise folding, the subsampling receiver with integrated filter before the subsampling mixer can be used. In terms of sensitivity and integration of the system, the balun-LNA based on the inductively degenerated structure is used to achieve high voltage gain and low noise figure. And it adopts the common-gate and common-source cascade topology to provide differential output signal. Moreover, the sampling frequency with high sampling ratio can be used to further reduce the power consumption. And quadrature sampling technique can acquire high energy efficiency. Therefore, the subsampling architecture with on-chip balun-LNA is proposed in this paper, which can achieve the quadrature sampling frequency conversion by low sampling frequency. This paper is organized as follows: a brief overview of related works is described in Section 2. And the theory analysis of it is introduced in Section 3. The proposed RF subsampling receiver and its building blocks are introduced in Section 4. The performance of the subsampling receiver is exhibited in Section 5. Finally, conclusions and discussion are drawn in Section 6.

2 Related works

Traditionally, an RF subsampling architecture can use a subsampling mixer to achieve frequency conversion, like a superheterodyne receiver. And it still adopts the synthesizer to provide sampling signal [13]. Moreover, a sampling clock jitter or high noise figure cannot be avoided, because of many folded noises emerging in the system. In addition, high sampling frequency with low sampling ratio used to down-convert RF signal to intermediate frequency or baseband, which can increase the complexity and power consumption of the system [22].

Nowadays, some new techniques, such as high Q filter and high sampling ratio, can be used to achieve high sensitivity, high integration, low noise, and low power consumption for the subsampling architecture [23]. For example, the subsampling receiver with band-pass anti-aliasing filtering can achieve lower power consumption and more flexible than direct conversion or low-IF receivers [24]. Usually, RF subsampling architectures include voltage sampling and charge sampling techniques [25]. Firstly, the charge sampling techniques adopt the charge charging and discharging to achieve frequency conversion, which has more advantages at phase linearity and clock jitter in high frequency and wideband fields [26]. For example, a reconfigurable IF to DC subsampling receiver architecture described in [27] targets 60 GHz band. And a cascaded charge-domain sampling mixer can achieve an 80-dB suppression of aliasing interferences while consuming 1.08 mA [28]. However, it is difficult to acquire high sensitivity and low noise figure with the charge sampling techniques, because of low voltage gain and many folded noises. And there are many charging capacitors used in the circuits, which can increase the complexity and size of the system. Recently, Xu et al. [29–31] proposed a crowdsensing-based wireless communication data processing methods and be proved with good performance.

While the voltage sampling architecture adopts the voltage value sampling and holding to achieve frequency conversion, which can be widely used in the narrowband systems [25]. For example, subsampling architecture for GPS receiver has been reported in [32], which has a low noise figure of 3.8 dB and noise figure loss after the subsampling mixer is less than 1 dB. However, the complexity and power consumption of the system can be increased by RF filter, which has a high gain of 25 dB. In order to further reduce power consumption of the receiver, high sampling ratio can be used in the subsampling receiver. As an example, subsampling mixer with integrated filtering, for an RF input frequency of 2.42 GHz with a sampling frequency of 100 MHz, achieves a high sampling ratio of 20 [33]. However, the parallel resonant LC filter with low Q cannot effectively restrain noise aliasing, which results in high noise figure. Moreover, RF signal can be translated to intermediate frequency or baseband by low sampling frequency,

which generates many folding noises in subsampling architectures [34]. Thus, bandpass filter before a subsampling mixer should be used to reduce the noise folding. As an example, a 2.4-GHz RF sampling receiver was reported with an input sampling rate of 1072 MS/s [35], which can fulfill the signal demodulation. However, the size and the power consumption of the system would be increased by high sampling frequency and complex down-conversion filter. And a high precision ADC is used to improve dynamic range of the system. Such as a continuous-time (CT) delta-sigma modulator (DSM) can demodulate signal for RF subsampling receivers, which can achieve high dynamic range of the modulator for OSR = 64 at the cost of high complexity of the system [36]. In order to achieve multi-channels and multi-standard applications, a flexible subsampling frequency can be adopted to down-convert RF signal to intermediate frequency or baseband. For example, multi-standard RF subsampling receiver architecture is reported in [37], which includes two subsampling stages: first stage with the fixed subsampling frequency and second stage by a tunable IF sampling frequencies clock. It can achieve frequency conversion for a GSM, UMTS, and IEEE-802.11g multi-standard receiver. However, a tunable bandpass RF filter and an IF bandpass filter increase the complexity of the system. In order to further improve the sensitivity and reduce the power consumption of the receiver, high sampling ratio and high Q filter can be used in the subsampling receiver. For example, a subsampling receiver can achieve −91 dBm sensitivity at 10^{-3} BER for pi/4-DQPSK modulation with low power [38]. However, Q enhancement with the tuning LNA can increase the complexity of the system. Taking the above problems into consideration, the detail analysis for the RF subsampling architectures should be introduced.

3 RF subsampling architecture and theory

3.1 Subsampling theory

The simple diagram of RF subsampling receiver is shown in Fig. 1, which includes a LNA, a subsampling mixer, and baseband demodulation blocks. The RF signal coming from antenna is filtered and amplified by LNA, and sampled and down-converted to baseband by the subsampling mixer, achieving subsampling frequency conversion. Finally, the baseband (BB) can fulfill signal demodulation in the digital circuits.

The frequency conversion of RF subsampling receiver is shown in Fig. 2; RF signal is transferred to low intermediate frequency f_{IF} by a proper local sampling frequency f_s [13], and further converted to baseband. There are some folding images existing into a frequency down-conversion process, which seriously interferes with the information signal [14]. In order to avoid folded images, a high Q filter should be used before a subsampling mixer. Moreover, it is very important to choose a sampling frequency for achieving the frequency down-conversion. According to the Nyquist Theorem, the local sampling frequency must be more than twice of the bandwidth of the information signal. Meanwhile, in order to avoid aliasing noises, the local sampling frequency should meet the following Eqs. (1) and (2) as follows:

$$f_s \geq 2 \cdot f_{\mathrm{signal}} \tag{1}$$

$$\frac{2f_{\mathrm{RF}} + f_{\mathrm{signal}}}{N+1} \leq f_s \leq \frac{2f_{\mathrm{RF}} - f_{\mathrm{signal}}}{N} \quad \mathrm{N} = 1, 2, 3, \ldots \tag{2}$$

where N is a subsampling ratio, f_{RF} and f_s are RF signal frequency and a local sampling frequency, respectively, f_{signal} is the bandwidth of information signal. From Eqs. (1) and (2), the local sampling frequency f_s is mainly determined by RF frequency f_{RF} and the sampling ratio N, as shown in Fig. 3. When f_{RF} is constant, the larger sampling ratio N is, the smaller the allowable local sampling frequency range is. However, a high sampling rate would increase the complexity of ADC. Thus, the local sampling frequency should be considered carefully. For the applications of IoT wireless communication, the subsampling receiver operates at the RF signal frequency f_{RF} of 780 MHz with the bandwidth of 20 MHz. At the data rate of 1 Mbps, the local sampling frequency f_s should be more than 2 MHz. Because of the allowable range of the local sampling frequency f_s, the sampling ratio N cannot be more than 50.

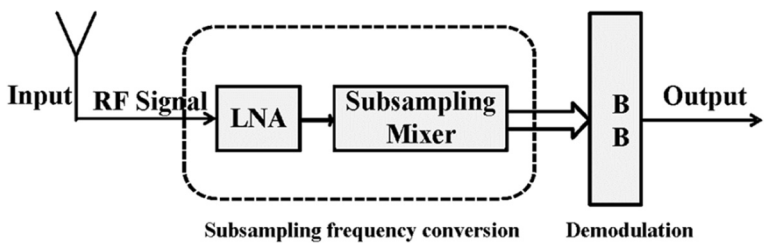

Fig. 1 The simple diagram of RF subsampling receiver, consisting of a low noise amplifier, a subsampling mixer, and baseband demodulation blocks

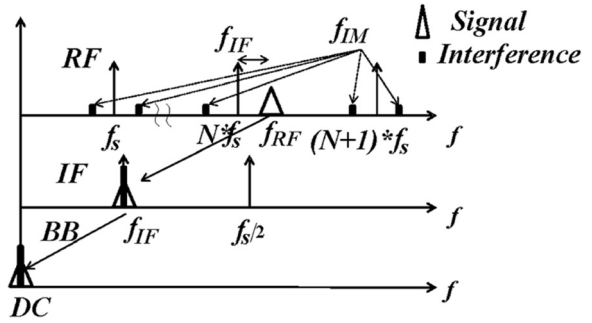

Fig. 2 Frequency conversion of the subsampling receiver (RF signal is transferred to low intermediate frequency by using sampling frequency, and then further converted to baseband signal)

In order to avoid DC drift and flicker noise of zero intermediate frequency architecture, the subsampling architecture samples and down-converts RF signal to low IF signal. Furthermore, it can be translated to quadrature I/Q path signal by one clock signal. And then the local sampling frequency is defined as follows:

$$f_s = \frac{4f_{\mathrm{RF}}}{2N-1}, \qquad N = 1, 2, 3, \ldots \tag{3}$$

The phase difference between adjacent samples ΔΦ is provided as follows:

$$\Delta\Phi = 2\pi\frac{f_{\mathrm{RF}}}{f_s} = (2N-1)\frac{\pi}{2}, \qquad N = 1, 2, 3, \ldots \tag{4}$$

From Eqs. (3) and (4), the intermediate frequency IF can be expressed as follows:

$$f_{\mathrm{IF}} = |f_{\mathrm{RF}} - H \cdot f_s|_{\min} = f_s/4 \;\; H = 1, 2, 3, \ldots \tag{5}$$

When S_{IF} is defined as the IF signal, the quadrature output at IF is provided as follows:

$$\begin{aligned} S_{I,M} &= S_{\mathrm{IF},M} \cdot \cos\left(2\pi f_{\mathrm{IF}} \cdot \frac{M}{f_s}\right) = S_{\mathrm{IF},M} \cdot \cos\left(\pi\frac{M}{2}\right) \\ S_{Q,M} &= S_{\mathrm{IF},M} \cdot \sin\left(2\pi f_{\mathrm{IF}} \cdot \frac{M}{f_s}\right) = S_{\mathrm{IF},M} \cdot \sin\left(\pi\frac{M}{2}\right) \\ & M = 1, 2, 3, \ldots \end{aligned} \tag{6}$$

where $S_{I,M}$ is I path IF signal, $S_{Q,M}$ is Q path IF signal. For example, based on the above equations from (3) to (6), the RF signal frequency f_{RF} is 780 MHz with the bandwidth of 20 MHz. When the sampling ratio N is 20, the local oscillation frequency is 80 MHz. The RF signal frequency f_{RF} can be down-converted to the intermediate frequency f_{IF} of 20 MHz. After a sample and hold (S/H) mixer, the intermediate frequency f_{IF} is classified into I path $S_{I,M}$ and Q path $S_{Q,M}$ by the odd I path samples and the even Q path samples, respectively, which can further reduce the sampling rate and relax the complexity of ADC.

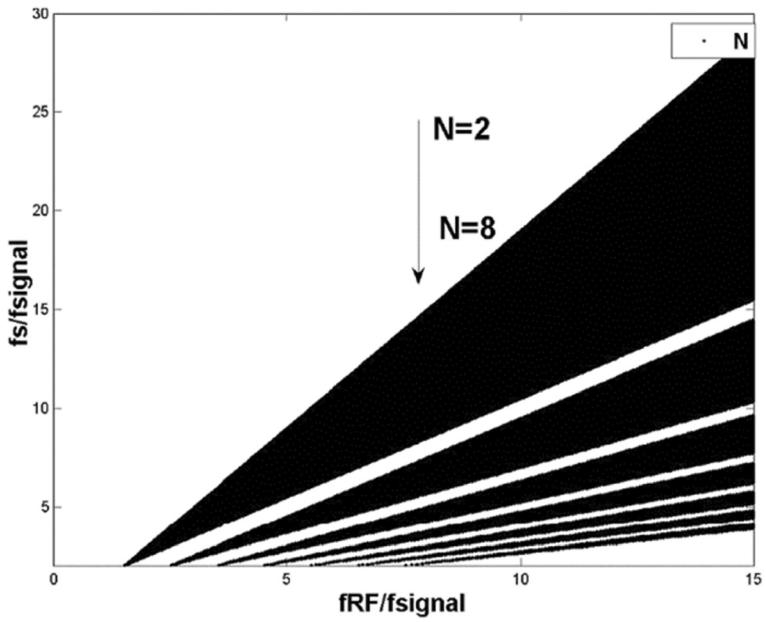

Fig. 3 Allowable range of sampling frequency shown in the shaded region (the large the sampling ratio N is, the small the allowable local sampling frequency range is)

3.2 Voltage sampling and charge sampling

Generally, RF subsampling receivers mainly include voltage sampling and charge sampling architectures. Regarding system architecture, sampling principle and noise figure, two different architectures are analyzed to distinguish their respective advantages and disadvantages. The diagram of the voltage sampling architecture is shown in Fig. 4, including an ideal voltage source, a sampling switch S, a capacitor C, and a resistance R [13]. The sampling impulse clock can control the switch, when the switch is ON, the sampling capacitor can sample and hold input signal voltage.

If input voltage signal is $V_{\text{in}}(t)$, output voltage $V_{\text{out}}(t)$ is given. Through Fourier transform, the frequency domain of the transfer function $H(f)$ is expressed as follows:

$$|H(f)| = \frac{\left|e^{-(j\cdot a\tan(2\tau\pi f))}\right|}{\sqrt{1+(2\tau\pi f)^2}} \quad (\tau = \text{RC}) \tag{7}$$

From (7), the translated frequency has a maximum at DC and nulls at the n times of f_s (n is integer), which can avoid the noise aliasing.

However, a diagram of charge sampling architecture is shown in Fig. 5, which includes an ideal voltage source, a transconductance stage G_m, a sampling switch S_s, a reset switch S_r and a capacitor C [27]. When the switch S_s is ON and S_r is OFF, the current translated by G_m is integrated into the capacitor C. And when switch S_r is ON and S_s is OFF, output signal can be discharged and reset. Taking the Fourier transform, the transfer function $H(f)$ of the charge sampling in frequency domain is defined as follows:

$$|H(f)| = \frac{G_m}{C}\left|\frac{\sin\left(\frac{\pi f}{2f_s}\right)}{\pi f}\right| \tag{8}$$

From (8), Sin () function only depends on the f_s, and the integration window of the charge sampling architecture can be depended on sampling ratio f/f_s. It has a maximum at DC and minimum at every multiple f_s.

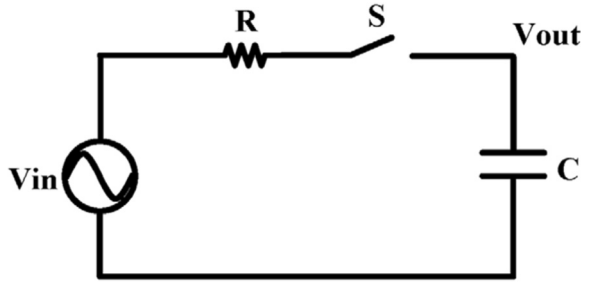

Fig. 4 The diagram of simple voltage sampling, including an ideal voltage source, a sampling switch *S*, a capacitor *C*, and a resistance *R*

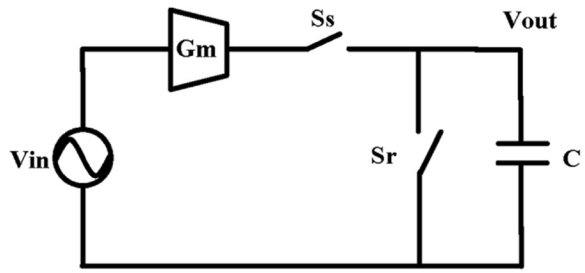

Fig. 5 The diagram of charge sampling, including an ideal voltage source, a transconductance stage G_m, a sampling switch S_s, a reset switch S_r, and a capacitor C

Based on the above different frequency response of voltage sampling and charge sampling techniques, the −3 dB bandwidth of voltage sampling circuit is determined by the time constant τ, while charge sampling architecture just depends on integral window width.

3.3 Noise analysis

There are two main noises: thermal noise and flick noise in the subsampling architecture. With more harmonic mixing of subsampling frequency f_s, noise folding would seriously affect noise figure of the system. In addition, the flick noise can be ignored in low-IF system.

In the voltage sampling architecture, thermal noise from S/H mixer is the main noise source. Comparatively speaking, others from ADC can be ignored. The equivalent noise of S/H mixer is expressed as follows:

$$\bar{V^2}n = \frac{kT}{C}\cdot\frac{1}{N} \tag{9}$$

where kT is thermal noise constant, N is the sampling ratio, and C is sampling capacitor.

In the charge sampling architecture, the thermal folded noise is also the main noise source. Since the bandwidth of the charge sampling architecture depends on the integral window width [26], noise power of thermal noise aliasing can be expressed as follows:

$$P_n = T_i\left(\frac{G_m}{C}\right)^2 \tag{10}$$

Except for the thermal noise aliasing, the flick noise is other noise factor, which is provided by

$$\bar{V^2}n = \frac{K}{C_{ox}\cdot W\cdot L}\cdot\frac{1}{f} \tag{11}$$

where K/C_{ox} could be regarded as the constant. Therefore, size of $W\cdot L$ and capacitor C can determine noises of the system.

According to the above analysis, the charge sampling architecture has more advantages in the high frequency and wideband receiver architecture. While the voltage

sampling capacitor and resistor can be smaller enough to achieve better integration and higher gain. In order to simplify the structure and improve the flexibility of the system, the voltage sampling architecture is good suitable for narrowband and low frequency fields, especially IoT application.

4 Subsampling architecture and circuits design

4.1 Subsampling architecture

The traditional subsampling receiver mainly consists of a low noise amplifier (LNA), a sample and hold mixer, a complex bandpass filter, a clock generation, and an ADC. Usually, a single-ended input signal can be transferred to differential signal by an off-chip balun, which increases the size of system. And the sample and hold mixer adopts simple MOS switches and sampling capacitors to achieve frequency conversion, generating serious nonlinear effects and charge injection. Moreover, it adopts a high local sampling frequency to down-convert RF signal to IF signal. Therefore, the clock generation is needed to provide the high clock sampling frequency, which increases the power consumption of the subsampling receiver. In addition, a clock generation based on high BAW resonators increases the size of the system.

For the requirements of wireless communication applications of IoT, such as low data rate, low power consumption and high integration, a subsampling receiver adopts a simple ASK modulation. In addition, a 1 bit ADC (such as comparator) can be used to demodulate baseband signal. Compared to traditional subsampling receiver, the proposed subsampling receiver architecture is shown in Fig. 6, which includes a balun low noise amplifier (balun-LNA), a two-stage passive sample and hold (S/H) mixer, an intermediate frequency amplifier (IFA), two down-conversion filters combined with a finite input response filter and an infinite impulse response filter, 1 bit ADCs and a clock generator. The balun-LNA not only achieves a high gain and a low noise figure, but also provides the differential output signal, without using the off-chip balun. And the two-stage passive S/H mixer adopting complementary switches and capacitors can sample and translate RF signal to IF signal, which reduces nonlinear effect and charge injection. In order to reduce folding noises, IF should be further filtered and decimated to baseband by down-conversion filters, and baseband is demodulated and processed in digital circuits. A clock generator can provide local sampling signal, which can be translated to the clock sampling signal by two frequency dividers and the decimated sampling signal by D flip-flop. With the control of clock signal, RF signal is translated to IF by the S/H mixer and further decimated to baseband by the down-conversion filters.

According to the above subsampling theory analysis, the local oscillation frequency is 80 MHz with a sampling frequency of 40 MHz, and the decimated sampling rate is 10 MHz. When RF input signal adopts ASK modulation at a data rate of 1 Mbps and ratio of minimum signal to noise $\mathrm{SNR}_{\min}$ is about 13 dB, the total noise figure NF of the subsampling receiver could be express as follows:

$$\mathrm{NF} = -(-174\mathrm{dBm} + 10\log\mathrm{BW} + \mathrm{SNR}_{\min}) + P_{\mathrm{sens}} \quad (12)$$

where BW is the bandwidth of filter, P_{sens} is the sensitivity of the subsampling receiver. From the expression (12), the total noise figure NF is determined by BW, $\mathrm{SNR}_{\min}$, and P_{sens}. When the sensitivity of the subsampling receiver is −85 dBm with the 2-MHz bandwidth of filter, NF is 13 dB. Therefore, NF should be less than 9 dB, considering 3~4 dB loss. In order to meet the requirements of high sensitivity, low noise figure, and low power of the system, the total power consumption of the

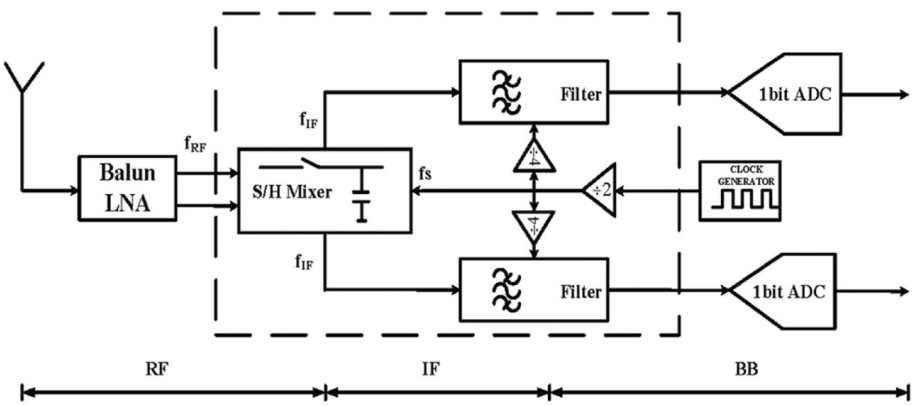

Fig. 6 The architecture of the proposed subsampling receiver. It consists of a balun low noise amplifier, a two-stage passive sample and hold mixer, an intermediate frequency amplifier, down-conversion filters, 1 bit ADCS and a clock generator

subsampling receiver should be less than 4 mW and the total voltage gain of the system cannot be less than 60 dB when the subsampling receiver achieves −85 dBm sensitivity at 10^{-3} BER. Further, with high noise figure of *S*/*H* mixer, the voltage gain of LNA should be more than 27 dB which reduces the total noise figure of the subsampling receiver.

4.2 Balun-LNA

In order to reduce the folding noise of the subsampling receiver, RF input signal should be filtered by the bandpass filter before *S*/*H* mixer. Although off-chip SAW/BAW filter can achieve high *Q* to filter the interference and reduce the anti-aliasing noises, it is difficult to improve integration of the system. By using the frequency selective network and choosing the proper sampling frequency, the folded noises can be reduced.

With restraining a common-mode noise and reducing parasitic couplings, differential configuration is widely used in the LNA circuits. However, off-chip baluns used to achieve differential signal, which degrades integration of the system. Traditionally, an active balun-LNA adopts the common-gate and common-source cascade topology to provide the differential signal output. However, it is difficult to achieve a high voltage gain and generate the differential signal of phase opposite and equal amplitude under process variation. Therefore, the proposed balun-LNA adopting the noise-cancelling technique is shown in Fig. 7, which can acquire a differential signal output. Firstly, transistor M1 achieves high gain and better input impedance matching, with the inductors L_s, L_g, and capacitor C_g. And then transistors M2 and M3 are consisted of the common-gate common-source differential output topology, achieving noise cancelling and distortion cancelling. A single-end RF signal is transferred from the drain of M1 to the source of M2 and the gate of M3 through the capacitor C_c, achieving differential output signal. Capacitor C_b provides AC coupling to ground and bias supply voltage makes enough current, which avoids using the larger inductor *L* to balance the current of differential output topology. As the first block in the subsampling receiving chain, the performance of the balun-LNA is of great importance, which can determine the noise figure and the power consumption of the whole system. Considering requirements of wireless communication for IoT application, the voltage gain of the balun-LNA should be more than 25 dB, and the noise figure and the power consumption of the balun-LNA should be less than 2 dB and 2.5 mW, respectively. Moreover, the amplitude and the phase mismatch of the differential signal output remains, respectively, within 0.5 dB and 5°.

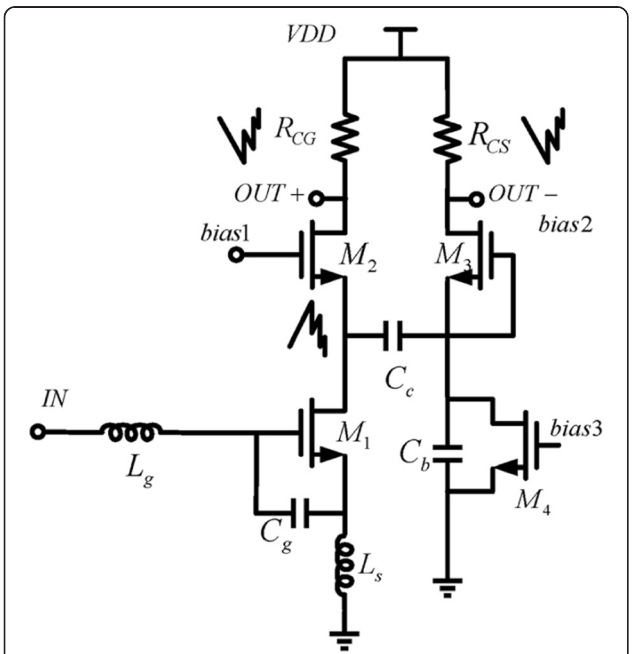

Fig. 7 Balun-LNA, including common-source single-ended input and common-gate common-source differential output topologies

In order to analyze the noise figure of the balun-LNA in detail, the noise figure of every stage of LNA is listed, respectively [16]. Firstly, the noise figure NF1of M1 can be calculated as follows:

$$\mathrm{NF1} = 1 + \frac{2}{\sqrt{5}} \cdot \frac{w\left(C_{gs1} + C_g\right)}{g_{m1}} \cdot \sqrt{\gamma\delta\left(1-|c|^2\right)} \qquad (13)$$

where the γ, δ, c are process parameters. NF1 is determined by the transconductance g_{m1} of M1 and the gate-source capacitance C_{gs1} and capacitor C_g.

Secondly, the typical CG–CS topology is widely used in LNA, which has been analyzed in detail [15]. The noise figure NF2 of the CG–CS topology can be calculated as follows:

$$\begin{aligned}\mathrm{NF2} = 1 &+ \frac{\gamma g_{m,CG} \cdot \left(R_{CG} - R_S \cdot g_{m,CS} \cdot R_{CS}\right)^2}{R_S \cdot A^2{}_{V,2}} \\ &+ \frac{\gamma g_{m,CS} \cdot R^2{}_{CS} \cdot \left(1 + g_{m,CG} \cdot R_S\right)^2}{R_S \cdot A^2{}_{V,2}} \\ &+ \frac{(R_{CG} + R_{CS}) \cdot \left(1 + g_{m,CG} \cdot R_S\right)^2}{R_S \cdot A^2{}_{V,2}}\end{aligned} \qquad (14)$$

Assuming that the transconductance $g_{m,CS}$ is *n* times bigger than the transconductance $g_{m,CG}$ and the load resistor R_{CG} is *n* times bigger than the load resistor R_{CS}, which can achieve the equal voltage gain. When transistor M3 is matched, R_S is the reciprocal of the transconductance $g_{m,CG}$ ($R_S = 1/g_{m,CG}$). Therefore, the noise

figure NF2 and the voltage gain $A_{V,2}$ of the CG–CS topology can be, respectively, rewritten as follows:

$$\mathrm{NF2} = 1 + \frac{4\gamma g_{\mathrm{m,CG}} \cdot \frac{R^2_{\mathrm{CG}}}{n}}{R_{\mathrm{S}} \cdot A^2{}_{\mathrm{V}}} + \frac{4\left(1+\frac{1}{n}\right)R_{\mathrm{CG}}}{R_{\mathrm{S}} \cdot A^2{}_{\mathrm{V}}} \tag{15}$$

$$A_{\mathrm{V,2}} = 2g_{\mathrm{m,CG}} \cdot R_{\mathrm{CG}} \tag{16}$$

where NF2 is determined by the transconductance $g_{\mathrm{m,CG}}$ of M3 and the load resistor R_{CG}. According to the impeding matching condition, the transconductance $g_{\mathrm{m,CG}}$ is 20 mS and the R_{S} is 50Ω. γ is about 4/3, and the load resistor R_{CG} is about 1000Ω so as to acquire high voltage gain. Based on the simulation of Eqs. (15) and (16) by using the Matlab, NF2 of the CG–CS topology is clearly shown in Fig. 8. The noise figure NF2 becomes smaller by increasing the transconductance ratio n ($n = g_{\mathrm{m,CS}}/g_{\mathrm{m,CG}}$). For example, when the transconductance ratio n is more than 4, NF2 of the system can be less than 1.5 dB. However, it is difficult to achieve transistors mismatching for higher n.

Considering impeding matching condition of CG transistor M3, the noise figure cannot be further reduced. However, based on the inductively degenerated stage, the proposed balun-LNA achieves the lower noise figure for the large R_{S} and small $g_{\mathrm{m,CG}}$. According to the cascaded formula of noise figure, the total noise figure of the balun-LNA can be expressed as follows:

$$\mathrm{NF} = \mathrm{NF1} + \frac{\mathrm{NF2}-1}{A_{V,1}} \tag{17}$$

Usually, the inductively degenerated cascade configured LNA has high voltage gain $A_{V,1}$. Therefore, noise figure NF1 has an important effect on the total noise figure NF of LNA.

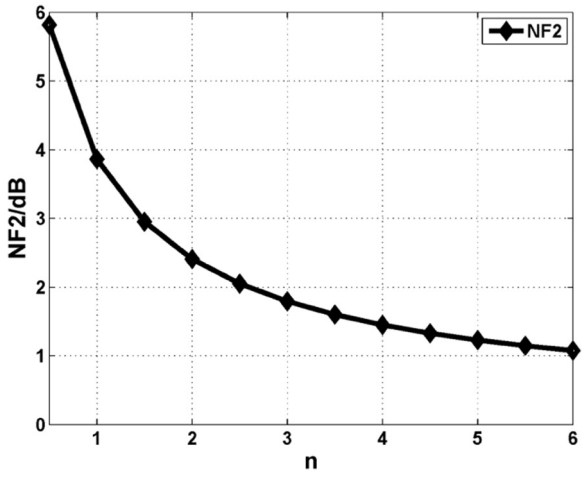

Fig. 8 Noise figure NF2 of the CG–CS topology for the transconductance $g_{\mathrm{m,CG}}$ is 20 mS, R_{s} is 50Ω, γ is about 4/3, and the load resistors R_{CG} is about 1000Ω

4.3 *S/H* mixer

Generally, differential sample and hold (S/H) mixer circuits include MOS switches and sampling capacitors. Without the high Q filter before S/H mixer, there are many folding noises affecting the information signal. In order to restrain the effect of folding noises, the proposed two-stage passive S/H mixer is shown in Fig. 9. Complementary switches constituted by NMOS and PMOS can reduce the charge injection. The differential output signal of the balun-LNA is sampled and converted to quadrature I path and Q path IF signals by the passive S/H mixer, respectively, without using high power-consuming RF PLL. However, after the first S/H mixer, RF interference signal still exists in the sampled signal. The second S/H mixer with the opposite clock sampling signal can be used to further fulfill the frequency conversion, which would relax the complexity of the following stages. Although the sampling capacitors should be large enough to reduce the kT/C noise, it would increase the size of the S/H mixer. Therefore, the sampling capacitor should be tradeoff between noise and size of the system. For the application of IoT, the clock sampling frequency of 40 MHz can be used with the sampling ratio of 20, based on the analysis of the sampling frequency. And the total noise figure of S/H mixer and second-order filter can be obtained as follows:

$$\mathrm{NF}_{\mathrm{mixer}} = \frac{S_{\mathrm{in}}}{N_{\mathrm{in}}} \cdot \frac{N_{\mathrm{out}}}{S_{\mathrm{out}}} \approx 1 + 3.3 \cdot \frac{N^2}{Q^2} + \frac{1}{2R_{\mathrm{s}} \cdot C_{\mathrm{s}} \cdot f_{\mathrm{s}}} \tag{18}$$

where Q is the quality factor and R_{s} is the resistor of an ideal voltage source, and NF is determined by C_s and f_s. Based on the simulation of Eq. (18) by using the Matlab, the total noise figure $\mathrm{NF}_{\mathrm{mixer}}$ of S/H mixer is clearly shown in Fig. 10. When Q is constant, noise figure becomes smaller by increasing sampling local frequency f_{s} or sampling capacitor C_{s}. However, the high sampling frequency f_{s} or large sampling capacitor C_{s} increases the complexity of the system. Therefore, it is of great importance to choose the proper local sampling frequency for the subsampling receiver. For example, the sampling capacitor C_{s} of 1 pF can be adopted for the system.

4.4 IFA and down-conversion filters

After frequency down-conversion of the S/H mixer, the weak IF signal should be amplified by the intermediate frequency amplifier (IFA). Traditionally, an operational amplifier (OPA) with resistance capacitance (RC) feedback used to amplify the IF signal, at the cost of increasing the size and the power consumption of the subsampling receiver. With two-stage

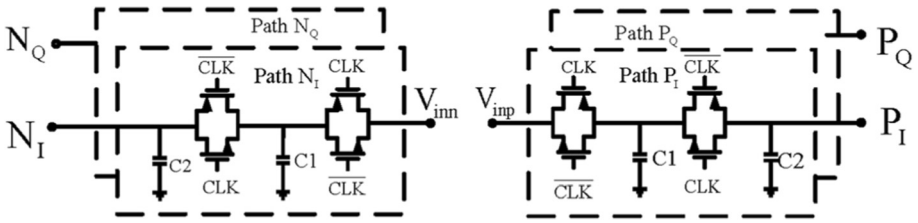

Fig. 9 Two-stage passive *S/H* mixer, consisting of complementary switches constituted by NMOS and PMOS and sampling capacitors

passive *S/H* mixer reducing folded noises, the schematic of the proposed single-stage IFA is shown in Fig. 11a, which is a simple two-stage amplifier. The input signal is amplified by the NMOS common-source amplifier with the current mirror load and the PMOS common-source amplifier with the resistive feedback [39]. IFA not only achieves the high voltage gain and reduces the power consumption but also acquires high isolation between the *S/H* mixer and the following stages. In addition, the resistive feedback configuration can improve the stability and provide enough phase margin which sacrifices a little noise figure of IFA.

In order to further reduce the folding noises emerging in the system, the typical complex down-conversion filters filter the frequency down-conversion signal. However, the lower the sampling frequency is, the smaller the orders of the down-conversion filters are. With the clock sampling frequency of 40 MHz for the subsampling receiver, the proposed discrete time filtering combined with finite input response (FIR) filter and infinite impulse response (IIR) filter is shown in Fig. 11b. For example, four-tap FIR filter mainly includes MOS switches and the sampling capacitors, which can achieve a high Q at the IF. Firstly, IF signal can be sampled and hold in capacitors $C_1 \sim C_4$ for a period. And then the sampled signal can be charged into the total capacitor C_5 and integrated into capacitor C_6 to output differentially, and the sizes of MOS transistors and sampling capacitors are the same so as to avoid the mismatch. Furthermore, FIR filter can transfer IF signal to baseband by using the decimated clock sampling signal. With the four-tap samplers, FIR filter can also achieve the function of bandpass filter, which has nulls at all multiples of sampling frequency and maximum at all odd multiples of intermediate frequency. And the decimating sampling rate becomes a quarter sampling frequency, which can relax the requirements of ADC. In addition, the transfer function *H(z)* of FIR filter is expressed as follows:

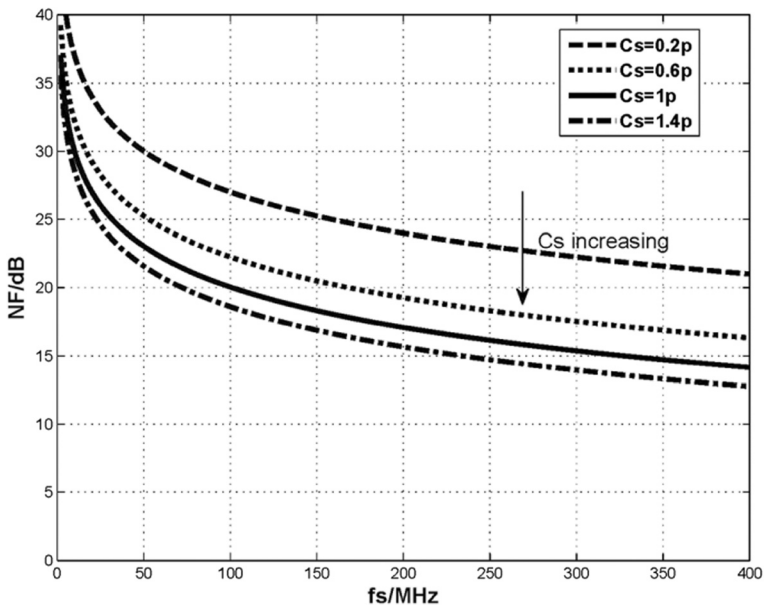

Fig. 10 Noise figure of subsampling mixer with sampling frequency or sampling capacitor increasing

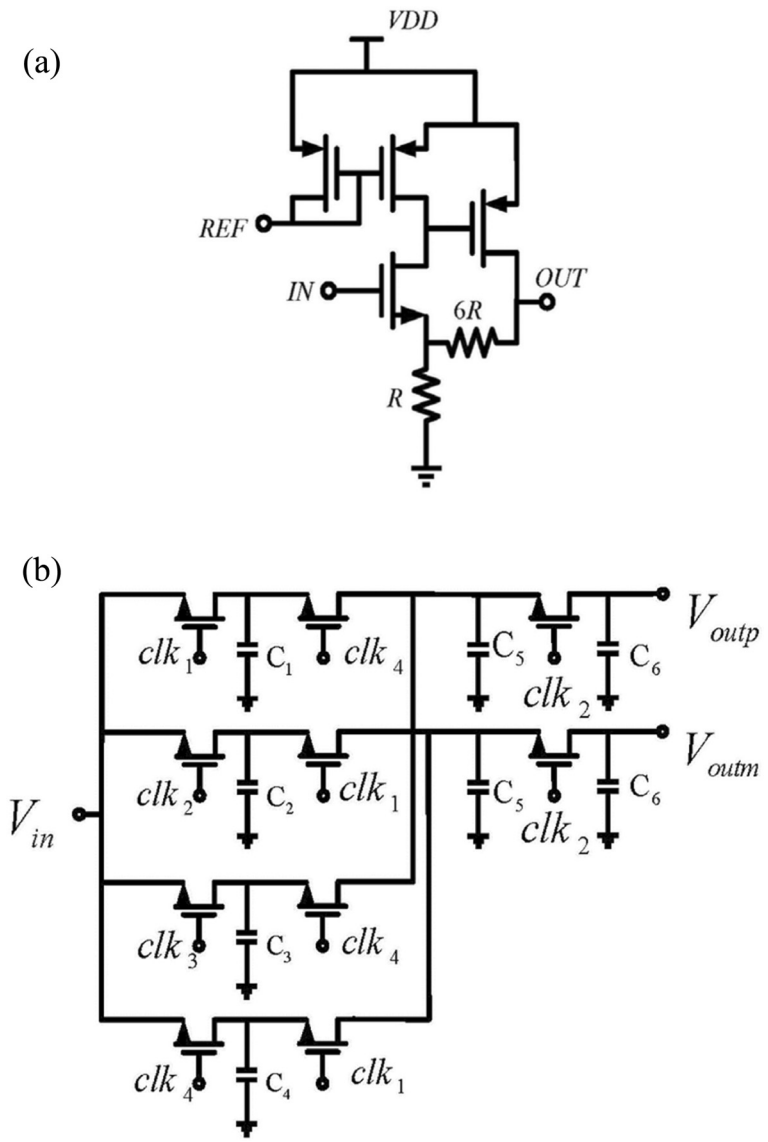

Fig. 11 Schematic of **a** IFA (constituted by the NMOS common-source amplifier with the current mirror load and the PMOS common-source amplifier with the resistive feedback) and **b** discrete time filtering combined with finite input response (FIR) filter and infinite impulse response (IIR) filter

$$H(z) = 1 - z^{-1} + z^{-2} - z^{-3} \qquad z = e^{jwT_s} \tag{19}$$

where T_s is the sampling cycle of four-tap FIR filter. The charge stored in the sampling capacitors can generate infinite impulse response (IIR), which has maximum at all multiples of sampling frequency and minimum at all odd multiples of intermediate frequency. Although the IIR filter reduces Q, it can still achieve maximum at all odd multiples of intermediate frequency.

4.5 Clock generator and 1 bit ADC

A clock generator usually adopts RF PLL to achieve the local sampling signal, which increases the complexity and the power consumption of the system. Therefore, the proposed clock generator has high integration and low power consumption shown in Fig. 12, which mainly includes the amplifier stages, buffers, and D flip-flop. Firstly, differential input signal can be shaped and amplified by the amplifier stages for LO signal. And then D flip-flops using the setting pulse excitation can generate the phased clock signal into $clk_1, clk_{1b}, \ldots, clk_{4b}$ with the buffers. The waveforms of clock sampling generator can be shown in Fig. 13, and $clk_1 \sim clk_4$ and $clk_{1b} \sim clk_{4b}$ can respectively decimate IF signal to quadrature I/Q output. To reduce the clock jitter, one clock is used to generate the clock sampling signal.

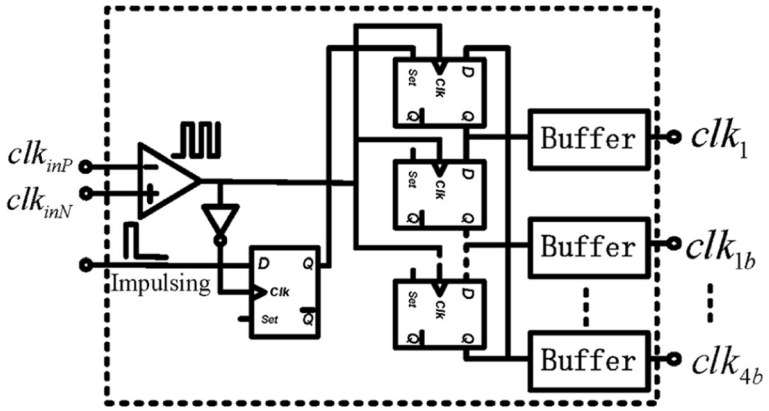

Fig. 12 A clock generator, mainly including the amplifier stages, buffers, and D flip-flop

Finally, an ADC, the last block in the receiver, is used to demodulate signal. For the subsampling receiver of IoT application, 1 bit ADC such as comparator can be adopted to demodulate the simple ASK modulation signal. In addition, parallel NMOS and PMOS differential pairs of comparator are adopted to demodulate the baseband.

5 System performance

The proposed subsampling architecture for the RF receiver is implemented, based on the transistor models of the United Microelectronics Corporation (UMC) 65 nm CMOS technology process by using the Cadence. In order to reduce the power consumption of the system, low threshold voltage NMOS and PMOS transistors were used to simulate the performance of the system-level. Because of many sampling capacitors in the subsampling blocks, especially discrete time filtering combined with FIR filters and IIR filters, the smallest size of sampling capacitor was used to reduce the size of the system. Therefore, the core die area of the subsampling receiver is 1.1 mm*0.9 mm, including *I*/*O* pads with ESD protected. For the application of IoT wireless communication, the proposed subsampling receiver operates at the RF signal frequency of 780 MHz with the bandwidth of 20 MHz and ASK signal at a data rate of 1 Mbps is used as the RF input modulation signal. The frequency down-conversion of the system can be achieved easily and flexibly by choosing the sampling frequency, based on input RF signal.

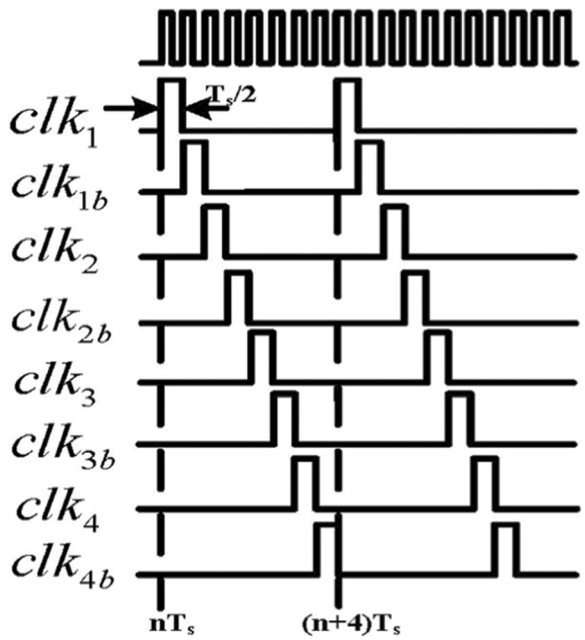

Fig. 13 Waveforms of clock generator and phased sampling clock, including the clock LO signal and decimated sampling signal

5.1 Current consumption

Based on the transistor models of CMOS process, the current consumption of the proposed subsampling circuits is simulated by using the Cadence. With the voltage supply of 1.2 V, the simulated results show that the total current consumption of the receiver is about 2.6 mA. And the current consumptions of the main blocks are listed in Table 1. Owing to lacks of high power-hungry blocks, such as RF PLL and high frequency LO, the proposed subsampling architecture achieves low current consumption. Moreover, the current consumption of the passive *S/H* mixer and FIR/IIR can be neglected. In order to further analyze the

Table 1 Current consumption of receiver

Blocks	Current
LNA	1.6 mA
S/H	1 μA
IFA	600 μA
FIR/IIR	100 nA
1 bit ADC	300 μA
Total	2.6 mA

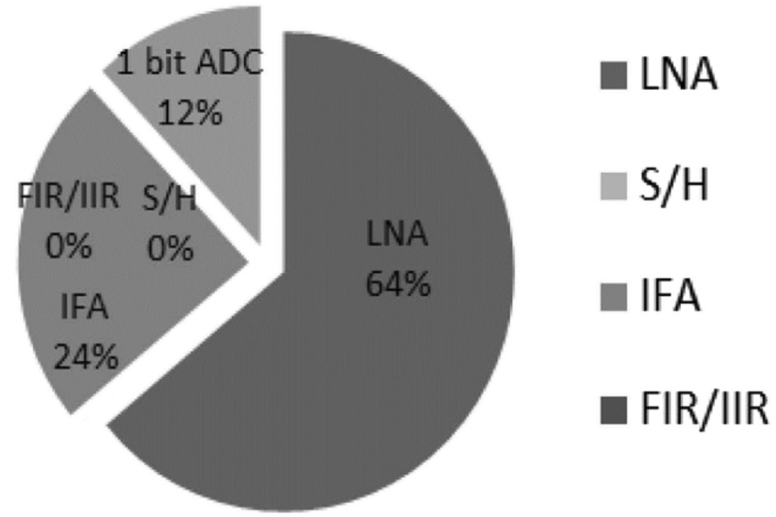

Fig. 14 Current consumption percentage of the subsampling receiver (current consumption percentage of balun-LNA, IFA, and 1 bit comparator respectively are about 64, 24, and 12 %, and others can be neglected)

current consumption of the main blocks, the current consuming percentage of every block is shown in Fig. 14. And the current consumption of balun-LNA is 1.6 mA, which is 64 % of the total current consumption of the system. Moreover, IFA and 1 bit ADC current consumption consumes, respectively, 0.6 mA and 0.3 mA, which is about 24 and 12 %. However, in order to reduce the power consumption of the subsampling receiver immensely, the power consumption of the balun-LNA should be reduced by using new architecture or low threshold voltage transistors, such as the supply voltage of 0.5 V.

5.2 S-parameters

The performance of the subsampling receiver can be largely determined by the balun-LNA. By the inductively degenerated structure, the balun-LNA is used to achieve high gain and low noise figure. Because of input impeding matching using larger inductor L, the impedance matching of the balun-LNA adopts the off-chip components. Based on the simulation of the LNA by using the Cadence, the results exhibit that S11 of LNA spacing from 550 MHz to 1.1 GHz is about −18 dB operating at 780 MHz as shown in Fig. 15. And the balun-LNA has a wider 3-dB bandwidth, which can meet the requirements of the signal transmission. In order to achieve differential signal of the equal amplitude and phase opposite, the gain and phase balance of the CG–CS topology of the balun-LNA are considered with the noise and distortion cancelling. Generally, the imbalance of the gain

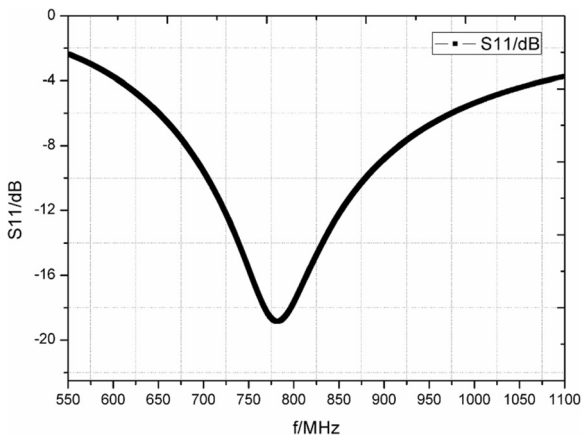

Fig. 15 Input matching S11 of LNA spacing from 550 MHz to 1.1 GHz, and −18 dB operating at 780 MHz

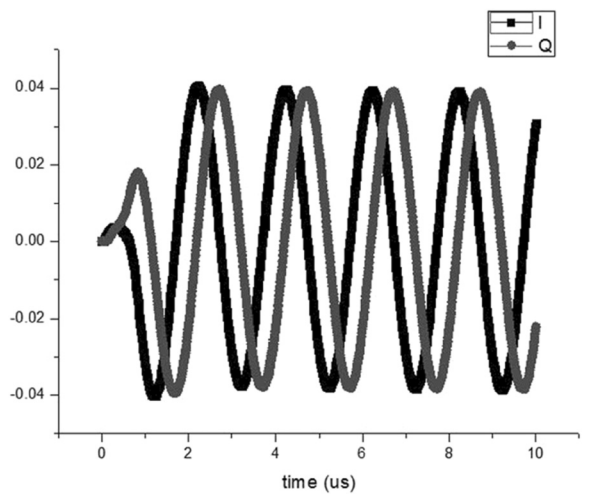

Fig. 16 The simulated quadrature output waveforms for input signal frequency of 780.5 MHz, and the clock sampling frequency of 40 MHz, input signal power level of −85 dBm and the output intermediate frequency of 500 KHz

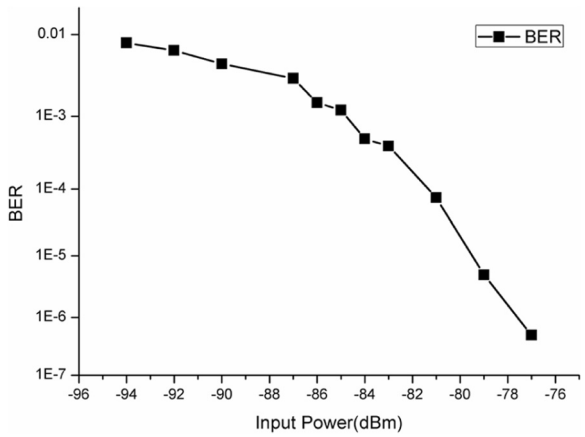

Fig. 17 Bit error rate for a different input power for the ASK modulation at a data rate of 1 Mbps (a range of input power level from −95 to −77 dBm)

and the phase of the balun-LNA are, respectively, within ± 0.5dB and ± 5°. According to the above analysis, the ratio n between the transconductance $g_{m,CS}$ and the transconductance $g_{m,CG}$ is 4, which can achieve a low noise figure. Moreover, the balun-LNA has integrated the bandpass filter before the *S/H* mixer to reduce the effect of folding noises.

5.3 System performance

According to analysis of the sampling frequency, the sampling ratio N between RF signal frequency and sampling frequency is very important to achieve frequency down-conversion. When input signal frequency is 780 MHz, a sampling ratio of 20 results in a sampling frequency of 40 MHz. RF signal frequency can be transferred to intermediate frequency of 20 MHz by the sampling frequency. And the four-tap FIR filter is used with the decimated sampling rate of 10 MHz, which has high Q at the intermediate frequency. Moreover, intermediate frequency is further down-converted to baseband by a decimated sampling rate. However, when input signal frequency is 780 MHz, a sampling ratio of 10 results in a sampling frequency of 80 MHz. RF signal frequency can be transferred to intermediate frequency (20 MHz) by sampling frequency. However, eight-tap or more complex FIR filter should be used to achieve high Q at the intermediate frequency, which increases the complexity of the down-conversion filter. In order to understand the frequency down-conversion of the subsampling receiver in detail, transient signal waveforms of the subsampling receiver is analyzed. If input signal frequency of 780.5 MHz is sampled by the clock sampling frequency of 40 MHz and input signal power level is −85 dBm, the output intermediate frequency is 500 KHz. The quadrature output waveforms of the subsampling receiver are shown in Fig. 16, based on the circuit simulation by using the Cadence. The time of transient waveforms is $10 \times e^{-6}$s. Further, the amplitude and phase mismatch of quadrature output signal remains respectively within 0.5 dB and 5°.

Considering the sensitivity of the subsampling architecture, system simulation of a bit error rate (BER) can be analyzed based on different input power levels. The subsampling receiver for the application of IoT adopts the ASK modulation at a data rate of 1 Mbps. Firstly, a pseudo random code source regarded as transmitted data can be generated by the Matlab, and the subsampling receiver can achieve frequency down-conversion and acquire demodulation signals with the Cadence simulation. And then different demodulated signals can be acquired according to different power levels of input signal. Compared to the transmitted data and demodulated data, the BER of the subsampling receiver is

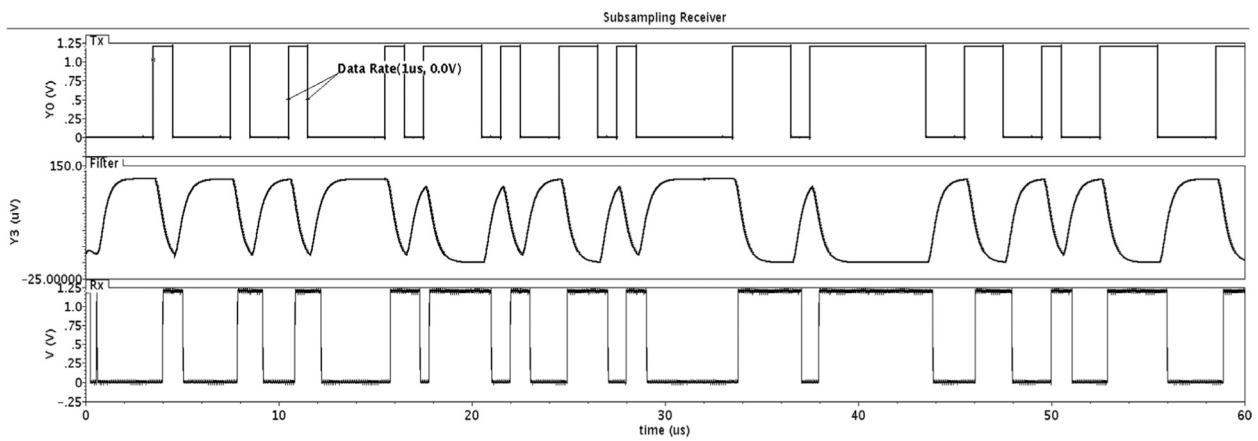

Fig. 18 Waveform of the transmitted and received signal for input signal frequency of 780 MHz, and the clock sampling frequency of 40 MHz, input signal power level of −85 dBm and a data rate of 1 Mbps

Table 2 Performance comparison

Reference	MWSCAS 13 [4]	JSSC 13 [10]	JSSC 13 [14]	ISSCC 14 [18]	JSSC 12 [21]	This work
Rx architecture	Direct IF	SDR	Subsampling	Low IF	Subsampling	Subsampling
Technology (CMOS)	65 nm	0.13 μm	0.18 μm	65 nm	0.18 μm	65 nm
Data rate	1 Mbps	1.5 Mbps	268 kbps	–	–	1 Mbps
Input frequency	780 MHz	915 MHz	2.433 GHz	860 MHz	2.4 GHz	780 MHz
Maximum gain	50 dB	54–60 dB	46.2 dB	50 dB	48 dB	67 dB
Noise figure	–	6.5 dB	8.6 dB	8.1 dB	–	6.5 dB
Sensitivity	−65 dBm	–	−78 dBm	–	−87 dBm	−85 dBm
Power consumption	4.5 mW (1.2 V)	5.03 mW (1.2 V)	10.69 mW (1.8 V)	1.15 mW (0.5 V)	8.84 mW (1.7 V)	3.12 mW (1.2 V)

analyzed and calculated by the Matlab. The sensitivity of the system is about −85 dBm for a BER of 10^{-3}, which is shown in Fig. 17. If using a high *Q* filter reduces the noise folding, the sensitivity of the system can be further improved.

In order to further exhibit the performance of the subsampling receiver, the waveforms of transmitted and received signal are exhibited in Fig. 18, and the time of the transient waveforms is $60 \times e^{-6}$s. When input signal power level is −85 dBm with input signal frequency of 780 MHz and the clock sampling frequency of 40 MHz, the maximum voltage gain of the whole system is 67 dB. In addition, noise figure of the system is about 6.5 dB by using the equation (12). The above waveform is the transmitted modulation signal with the data rate of 1 Mbps, and then the following waveform is baseband signal down-converted by *S/H* mixer and filtered by the discrete time filtering combined FIR and IIR. The last waveform is the demodulation output signal. In addition, the information signal can be recovery from the demodulated signal by using the clock sampling signal.

The comparison of the proposed receiver with other receivers is listed in Table 2. The subsampling receiver has higher gain and lower noise figure, while still consuming low power. Thanks to the balun-LNA with the noise-cancelling technique and four-tap FIR filter, the noise figure of the system is improved.

6 Conclusions

The proposed subsampling architecture for the RF receiver achieves frequency down-conversion and signal demodulation for wireless communication applications. From the aspects of system architecture, sampling principle and noise figure, the proper clock sampling frequency of 40 MHz is used to transfer the RF signal to the quadrature *I* path and *Q* path IF signals, respectively, at low power operation. Moreover, the balun-LNA and the passive *S/H* mixer without using RF PLL can guarantee high voltage gain and low noise figure of the subsampling architecture. Considering other performances, such as power consumption, voltage gain, noise figure, and sensitivity, the proposed architecture is well suited for the narrowband wireless communication applications. Further, low voltage supply and the advanced CMOS technologies reduce power consumption of the system significantly.

The noise figure of the system is further improved by using the *Q* enhancement technique. Although the receiver has already exhibited good performance with the simple ASK modulation and the sampling ratio of 20, more advanced modulation and the higher sampling ratio can be used to further improve the performance of the system.

Competing interests
The authors declare that they have no competing interests.

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