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Research Article

A Potential Transmitter Architecture for Future Generation Green Wireless Base Station

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Current radio frequency power amplifiers in 3G base stations have very high power consumption leading to a hefty cost and negative environmental impact. In this paper, we propose a potential architecture design for future wireless base station. Issues associated with components of the architecture are investigated. The all-digital transmitter architecture uses a combination of envelope elimination and restoration (EER) and pulse width modulation (PWM)/pulse position modulation (PPM) modulation. The performance of this architecture is predicted from the measured output power and efficiency curves of a GaN amplifier. 57% efficiency is obtained for an OFDM signal limited to 8 dB peak to average power ratio. The PWM/PPM drive signal is generated using the improved Cartesian sigma delta techniques. It is shown that an RF oversampling by a factor of four meets the WLAN spectral mask, and WCDMA specification is met by an RF oversampling of sixteen.

1. Introduction

The existing third generation network deployed around the world is not sufficient to meet the needs of new upcoming bandwidth intensive applications. It is expected that by 2012, two-thirds of the estimated 1.8 billion broadband users will be connected through a wireless device [1]. A fourth generation wireless system will be required to transmit higher bit rates to more users in a more flexible way. This will lead to higher transmission bandwidths and greater transmission powers. Transmission efficiencies must therefore increase if the equipment is to be housed in existing shelters, using existing cooling (air-conditioning) and existing power sources.

Mobile operators around the world are becoming increasingly interested to reduce their operating costs and carbon footprint. Developing countries are particularly susceptible because of the low income of their subscribers. Therefore, base station manufacturers around the world are looking for solutions to develop "greener" and efficient technology. The goal here is to replace the power connection (or diesel generator in developing countries) with solar cells. This is only practical if the overall basestation power consumption can be reduced to realistic levels. At present, the radio frequency power amplifier (PA) is the largest power usage component, accounting for approximately 30%–40% of a 3G wireless base station's total consumption. High power usage leads to higher costs and an unacceptable environmental impact.

Efficient multicarrier schemes such as orthogonal frequency division multiplexing (OFDM) are required to cater for the increasing transmission bandwidths. OFDM signals require conventional linear PAs. A tradeoff between efficiency and linearity always exists in PA design. A typical feed-forward class AB PA has efficiency in the range of 10% with modulated signals. Alternatively, a class E switched mode PA has the potential to attain drain efficiencies of up to 45% when operated with 8 dB peak to average Rayleigh enveloped signal [2]. Switch mode power amplifiers (SMPAs) are highly nonlinear and attain maximum efficiency if driven

by a pulse waveform. The challenge is on the modulation stage to generate the appropriate drive signal which is optimised for efficiency and linearity. This has lead to a renewed interest in architectures such as linear amplification with nonlinear components (LINCs), envelope elimination and restoration (EER), and pulse width modulation (PWM) [3–5]. This paper considers a combined EER and PWM amplifying scheme.

The continuing improvement in silicon technology is enabling digital circuits to operate at higher frequencies suggesting that direct digital generation of the amplifier's RF drive signal is now possible. Figure 1(top) shows the traditional wireless base station architecture and a proposed architecture (Figure 1(bottom)) for a future generation of wireless base stations using SMPAs (e.g., classes D and E). The new architecture eliminates most analog components in the driver circuit. These include digital to analog converters (DACs), reconstruction filters, the local oscillator, and the quadrature modulator. The new all-digital architecture can thus be easily integrated on chip.

The EER-driven PA architecture, Figure 1(middle), has a theoretical efficiency of 100% and operates by splitting the signal into polar components (envelope and phase). The envelope, u, controls the SMPA supply and the phase, s, controls the pulse position modulator of the input pulses which form the RF drive signal. This is a constant envelope modulated signal that keeps the amplifier operating in its most efficient saturated mode. However, this structure suffers from bandwidth expansion when used with OFDM signals. OFDM is a noise-like signal with a random path in the I and Q plane, any near zero crossings cause large dips in the envelope signal and a large rate of phase change (instantaneous frequency) for the phase drive signal. The coordinate transform of the OFDM signal from Cartesian to polar therefore results in envelope and phase components that have wider bandwidths than that of the input signal. Unfortunately, the bandwidth of the polar envelope component cannot be too high since sharp dips in the magnitude cannot easily be reproduced by the switch mode DC-DC converter. We therefore propose a technique to reduce the envelope's bandwidth expansion without distorting the output signal (Figure 1(bottom)). Bandwidth reduction is possible by allowing some amplitude variation in the phase signal, s, driving the amplifier. The amplitude variation can be impregnated onto the phase modulated pulse position modulation (PPM) signal, $s_{\Sigma\Delta}$, by applying pulse width modulation (PWM) on the PPM pulses of the input RF drive signal (Figure 2). This maintains the all-digital architecture. If synchronous digital circuits are to be used the pulse edges must occur on the timing grid of the digital clock. This limits the selection of possible pulse positions and pulse widths leading to time quantisation. Sigma delta ($\Sigma\Delta$) converters can generate the two state PWM/PPM signal, while shaping the time quantisation noise away from the band of interest.

In this paper, we measure the output power and efficiency of a GaN single stage amplifier and from these results we then predict the performance of the amplifier in the new architecture. We show there is a tradeoff between amplifier efficiency and the bandwidth of the envelope component. Section 2 compares the efficiency of a GaN amplifier operating in two modes; the first mode uses an approximate PWM gate drive signal and the second mode uses a high level EER drive on the V_{dd} supply line. Section 3 introduces a new technique for bandwidth reduction of the polar envelope drive signal and then predicts the efficiency based on the amplifier measurements. Section 4 discusses the use of ($\Sigma\Delta$) to generate a suitable amplifier input pulse train with phase and amplitude information encoded in its pulse width and pulse position. Section 5 concludes by discussing the viability of the new architecture.

2. Switch Mode Power Amplifier

In this section, we predict from measurements an amplifier's performance in two operating modes. The first mode uses a PWM [6] drive signal and the second mode uses the more conventional polar EER drive signals. The operating frequency of the power amplifier is designed to be 400 MHz. A discrete GaN HEMT device is chosen because it has good gain at high power and a lower drain-source capacitance than competing LDMOS devices which should make it more suitable for high efficiency in switch-mode operation [7].

2.1. PA with PWM Drive and EER Drive. A simple way to obtain PWM operation is to use a comparator and a triangular drive signal with the reference input controlled by the envelope modulation (Figure 3). In this work the PWM signal is directly generated in the output power device to avoid the need for special wideband input matching circuits. The amplifier input is overdriven with the phase modulated sinusoidal carrier signal (V_p), and the gate bias (V_{bias}) is controlled by the envelope component of the modulated signal. Since the device threshold voltage (V_T) is fixed, this has the effect of varying the on/off duty cycle of the amplifier, as illustrated in Figure 4. The PWM like signal at the drain of the device has a slightly reduced slew rate because of the limited gain of the device. Also, the pulse width is no longer linear with respect to the envelope signal, $\Delta V = (V_T - V_{\text{bias}})$, because of the nontriangular drive signal. The latter indicates the need for linearisation. The output tuning network provides filtering of the pulsed drain signal and performs the impedance transformation from the load impedance to the drain of the device. The output and input networks were optimised for a range of pulse widths by simulation using the harmonic balance method of ADS [6].

The same amplifier configured as an EER PA structure is shown in Figure 5. Here the low frequency envelope signal modulates the PA supply (V_{dd}).

2.2. Measurement Results. The full amplifier including matching networks is implemented using surface mount components on a standard FR4 PCB, with double sided copper layers as illustrated in Figure 6. The inductor at the drain of the device is implemented using a transmission line. The device is a CREE CGH40010 discrete GaN HEMT device suitable for high output power (10 W), high efficiency (60%), and high frequency (6 GHz) operation. The threshold

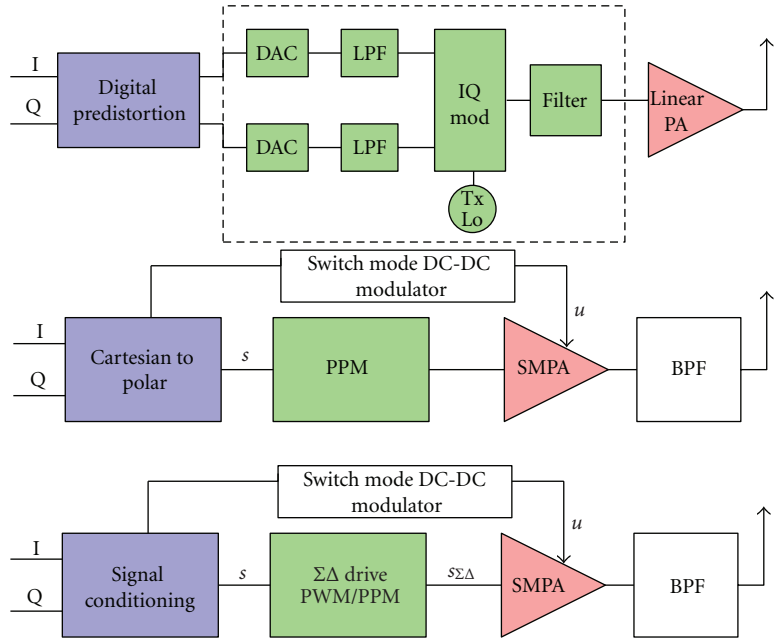

Figure 1: Traditional (top), EER (middle), and proposed (bottom) transmitter architectures.

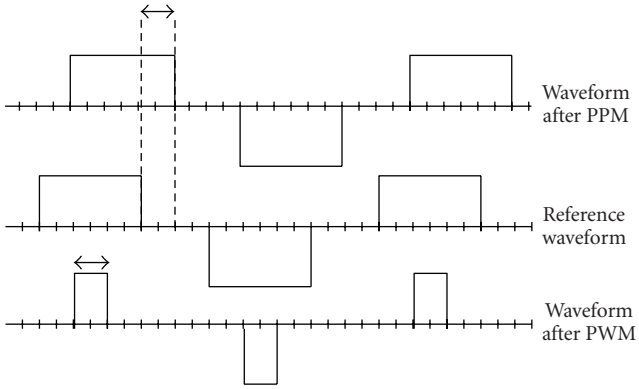

Figure 2: Demonstrating PWM (amplitude modulation) and PPM (phase modulation) concept. Edges occur on the digital timing grid.

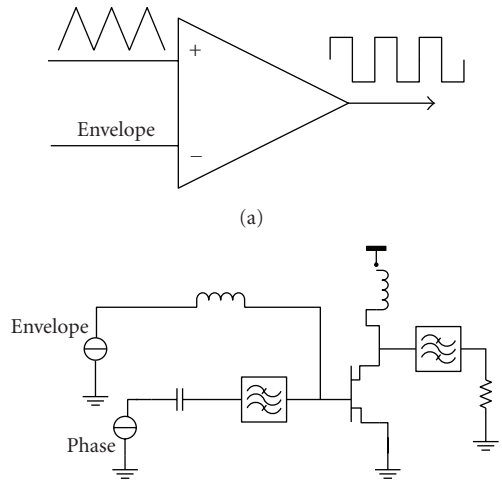

Figure 3: PWM generation: (a) ideal, (b) PA schematic.

voltage is −2.5 V, and the nominal supply voltage is 28 V [7]. The carrier frequency was 395 MHz and a high-power input signal was used (23 dBm), since the PA was to operate in switch-mode.

In Figure 7(a), the efficiency and output power as a function of V_{bias} are shown. The figure shows that the useful range of gate bias voltage is roughly 4 V, from −5 V to −1 V. This results in an output power variation from 19 dBm to 39.6 dBm, and a drain efficiency variation from 6% to 61%. The loss of efficiency at low output powers is consistent with PWM operation, where slew-rate losses are essentially constant whatever the pulse width (output power).

The EER architecture was not assembled fully, but measurements were made on the PA varying the supply voltage (V_{dd}) and keeping the gate bias voltage constant. The efficiency and output power are plotted in Figure 7(b). V_{dd}

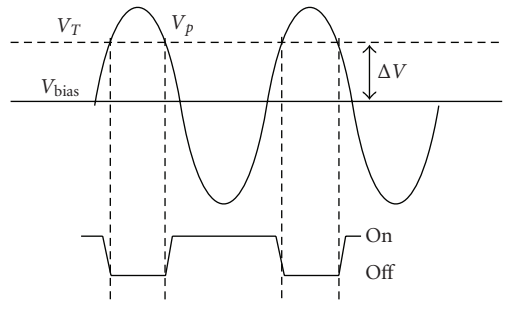

Figure 4: Operating principle of the power amplifier. The difference ΔV between V_{bias} and V_T varies, depending on V_{bias} and the resultant PWM drain signal is illustrated.

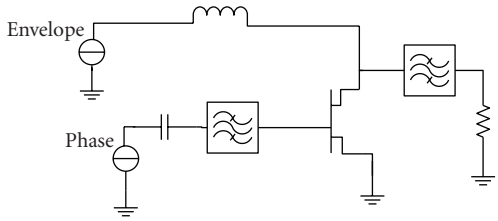

Figure 5: EER architecture.

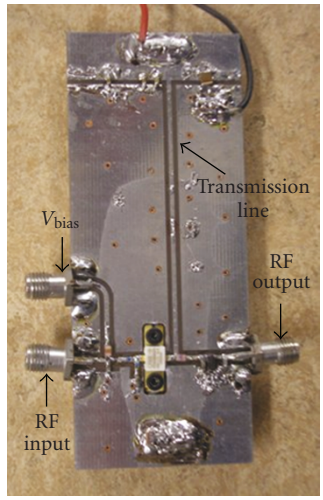

Figure 6: The PCB with the transmission line inductance and I/O ports indicated.

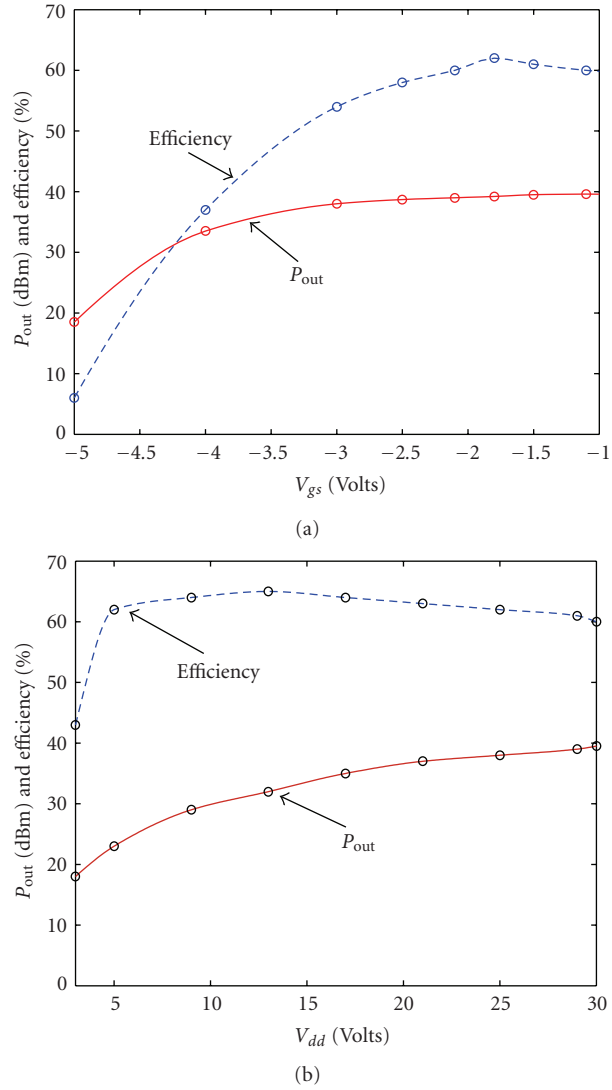

Figure 7: Measurement results. Output power and drain efficiency for (a) PWM-like operation and (b) EER operation.

scales the output signal, for example, doubling the supply voltage will increase the amplifier's output by 6 dB.

Comparing the efficiency performance of both the PWM and EER PA architectures, it can be noticed that with the PWM structure the efficiency holds good only over a small dynamic range, within less than 3 dB of peak output power. Therefore, to maintain high efficiency the amplitude variation needs to be small. On the other hand, the EER structure maintains efficiencies above 60% over a wide dynamic range (18 dB). Figure 8 restates the measured results in a way that gives a more insightful comparison. The plot shows the efficiency versus normalised output power for both architectures. The power is normalised to the amplifier's peak output power; in this case 39.6 dB for V_{dd} = 30 V. The dotted PWM curve is for measurement data with V_{dd} = 10 V. It has the same basic shape as the V_{dd} = 30 V curve, except for a small efficiency scaling due to the improvement in efficiency at lower V_{dd}'s (Figure 7(b)). The similarity between the normalised V_{dd} curves will be used later in the paper to calculate the expected efficiency of amplifiers using a combination of PWM and EER modulation.

Although, the EER architecture gives better efficiency with modulated signals it still requires a supply modulator, commonly implemented as a class-S amplifier. The switching frequency of the supply modulator must be considerably larger than the envelope bandwidth to minimise distortion; this increases the switching losses when the bandwidth is high. Therefore, a suitable bandwidth limitation scheme needs to be applied to the envelope component in order to maintain the supply modulator efficiency. The next section describes the trade-off between envelope bandwidth and amplifier efficiency.

3. Bandwidth Limitation

In the EER architecture, Figure 1(middle) generates the envelop signal for the DC to DC converter and a constant amplitude phase modulated signal for the amplifier input RF drive. The coordinate transform from Cartesian to polar results in signal components that have wider bandwidth than that of the original input signal. We propose a technique to reduce the bandwidth expansion of the envelope polar drive signal by using both EER and PWM/PPM modulation as shown in Figure 9. The amplifier effectively scales

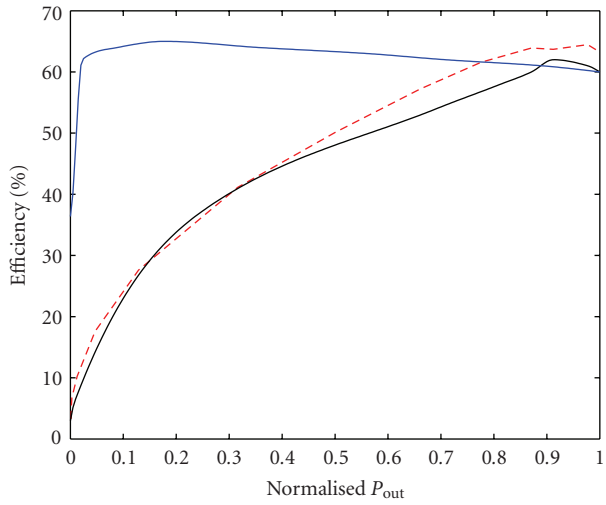

FIGURE 8: Efficiency against power output. PWM curves are for V_{dd} = 30 V (solid) and for V_{dd} = 10 V (dashed) and EER (solid).

(multiplies) the PWM/PPM output by the instantaneous V_{dd}.

The process first limits the envelope bandwidth, R, in a low pass filter and then adds a DC offset to stop clipping at the amplifier. The $u = R' + dc$ signal acts as the supply modulator for the amplifier. The phase information is obtained by dividing the input signal with u. Here, $s = x/(R' + dc)$ is the drive signal for the PA. The ΣΔ operation converts the magnitude/phase information of s into an equivalent PWM/PPM pulse driver signal $s_{\Sigma\Delta}$ for the amplifier. In the case of no bandwidth limitation (i.e., LPF bandwidth = ∞ Hz), the input drive, s, is a constant magnitude signal containing phase information only. The architecture then works as EER. On the other hand, if there is full bandwidth limitation (LPF bandwidth = 0 Hz), u contains only a fixed DC value and s is the original input signal, x. Limiting the envelope bandwidth and allowing some envelope variation into the phase drive signal, s, result in reduced bandwidth expansion for both envelope and phase drive signals. The input drive, s, is scaled multiplied by the envelope signal, u, within the amplifier to recreate, x, at the amplifier output.

Figure 10 shows the spectra of the OFDM RF signal, x, and its polar drive components s and R. The effect of envelope bandwidth limitation is shown with and without compensation of the phase drive signal. The thin solid lines show the RF and polar components, when there is no bandwidth limitation. This is the EER condition and clearly shows the bandwidth expansion of the envelope and input signals.

The dashed line, x, shows the blow out of the RF spectrum when the envelope (R', shown dotted) is bandwidth limited, to one OFDM channel without applying the corresponding compensation. Adjacent channel power exceeding −40 dBc will exceed the spectrum transmission mask for most standards (WLAN@ −40 dB and UMTS@−50 dB). The OFDM inband signal is also affected by a build up in error vector magnitude (EVM); but at a level of −38 dB, this is unlikely to cause a problem. When compensation is applied to the input signal, s, its bandwidth reduces (Figure 10 dotted), and the blowout in the RF spectrum is repaired, as is the EVM. The new architecture leads to envelope and input bandwidths being reduced to 28% of the original EER bandwidths, when measured at a −50 dB threshold. Even though the RF signal suffers no EVM or adjacent channel interference (ACI), when the envelope bandwidth is limited, the amplifier efficiency is compromised. We use the measured curves of Figure 8 to predict the amplifier efficiency when it passes an OFDM signal. This noise-like signal has a wide dynamic range and in the simulations amplifier clipping occurs when $R' + dc < |x|$, or if $|s| > 1$. Low DC values increase clipping but are best for efficiency. For each bandwidth limit we choose the DC value to give the same clipping energy as a normal OFDM signal clipped to 8 dB PAPR (peak to average power ratio). The clipping noise for each simulation is therefore the same.

Figure 11 shows the predicted efficiency versus envelope bandwidth plots for OFDM modulation. When there is no envelope bandwidth limitation the amplifier structure works as EER and the efficiency is at 62%. However, when the bandwidth limitation is at 0 Hz, that is, the envelope has only a fixed dc value, the efficiency is at 28% which is the efficiency of the PWM amplifier by itself. A further 10% efficiency can be gained with the envelope filtered to 0.25 channel bandwidths. The optimal point lies at the knee of the curve at 0.75 channel bandwidths which yields a 57% efficiency.

4. Pulse Train Generation Using Sigma Delta Modulation Technique

Figure 12 shows the block diagram of an architecture proposed in [8] which we refer to as Cartesian ΣΔ. It can generate a PWM/PPM pulse train with the appropriate phase and amplitude information, while having full compatibility with synchronous digital circuit design. It consists of two first-order lowpass sigma delta modulators (MOD 1 [9]), amplitude and a phase quantisers, and a polar to "PWM/PPM" block. The Cartesian signals pass through ΣΔ filters, after which they are converted to polar $[R, \theta]$ for quantisation in blocks Q_R and Q_θ. The quantised signals $[\hat{R}, \hat{\theta}]$ are then reconverted to Cartesian before being fed back to the ΣΔ filters. ΣΔs shape the quantisation noise away from the signal band. The previous reported structures perform ΣΔ filtering on the polar signal [10], while this work gives superior performance because the ΣΔ filtering is on the Cartesian signal where there is no bandwidth expansion. The equations from [11] are used to decide the amplitude threshold levels as the quantisation is performed in the polar domain. In this case, the amplitude is quantised into $(n/2 + 1)$ levels corresponding to pulse widths $(0, 2/n, 4/n, 6/n \cdots (n/2)/n)(1/f_c)$ (f_c = carrier frequency) and the phase is quantised into n phase increments from zero to 2π. This quantisation process requires the system digital clock to oversample f_c by a factor of n ($f_{\text{clock}} = nf_c$).

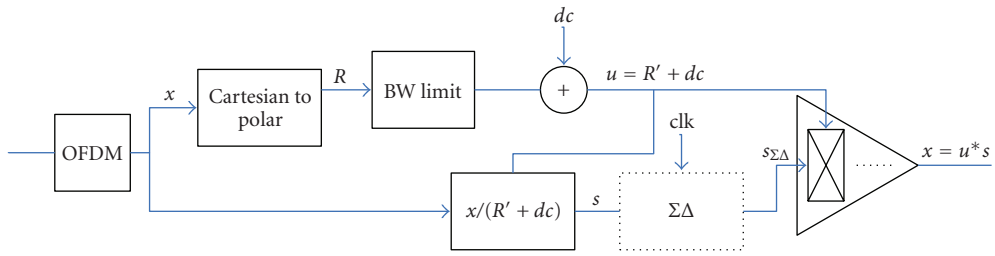

Figure 9: The new transmitter architecture. The ΣΔ clk operates at the carrier frequency and gives an amplitude and phase output for each RF cycle.

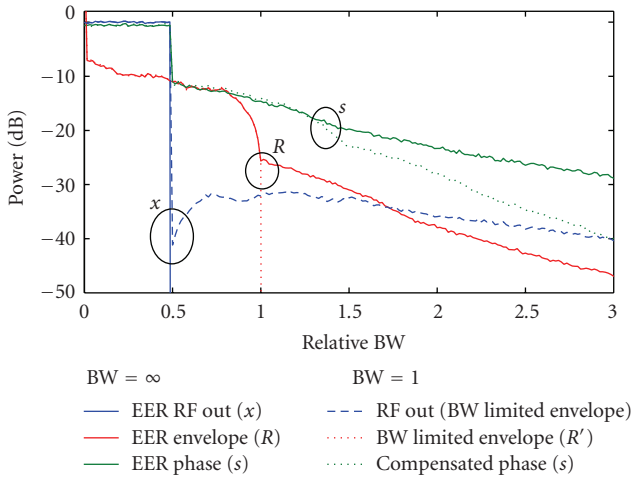

Figure 10: Spectra of the input drive signal, s, envelope signal, R, and RF signal, x.

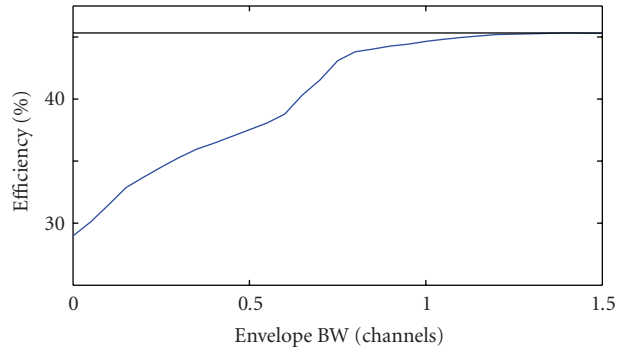

Figure 11: Average efficiency versus envelope bandwidth for an OFDM signal.

The "polar to PWM/PPM" block is responsible for upconverting the output of the quantisers to RF. The quantised phase, $\hat{\theta}$, determines the pulse position and the quantised amplitude, $\hat{R}$, determines the pulse duration [8]. The output of the "polar to PWM/PPM" block is a pulse train to be fed to the switch mode PA and band-pass filtered to eliminate quantisation noise and out-of-band distortion products.

A simulated OFDM signal was used to test the system described. In the spectral domain, the noise in the adjacent channels needs to be below an acceptable level. The out-of-band distortion products are measured by calculating the adjacent channel power (ACP) ratio, defined as the noise power in the adjacent channel over signal power. Figure 13 shows a spectrum plot of the Cartesian sigma delta at an input power of −7 dB. ACP1 indicates the first adjacent channel and ACP2 indicates the second adjacent channel. The shaping effect of the ΣΔ filters can be observed from the gradual increases in noise power as we move away from the band of interest. The output band-pass filter will limit any unwanted noise far away from the desired band.

Since the oversampling factor, n, has a direct impact on possible carrier frequencies, it is crucial to keep n as low as possible. Figure 14 shows a plot of ACP versus n. The appropriate n can be chosen depending on the spectrum mask of the standard. The Cartesian ΣΔ clearly outperforms the polar ΣΔ, leading to a lower n requirement for the same ACP. The results shown here for $n = 4$ are reasonable for the WLAN standard (ACP < -40 dB). However a higher oversampling rate of $n = 16$ is required to meet the tougher −50 dB WCDMA spectrum mask, limiting f_c to about 200 MHz using current digital technology ($f_{\text{clock}} = 3.2$ GHz). Clock rates must further improve before carrier frequencies in the cell phone bands can be handled.

5. Conclusion

A high efficiency all-digital transmitter architecture that uses a combination of EER and PWM/PPM modulation is described. We predicted the performance of this architecture from the measured output power and efficiency curves of a GaN amplifier. An OFDM signal limited to 8 dB PAPR will give 57% efficiency which compares favourably to the peak amplifier efficiency of 64% with a continuous wave signal (Figure 7).

A number of challenges still exist before a high efficiency all-digital transmitter can be realised at high carrier frequencies. From the amplifier perspective parasitic capacitances will always limit the efficiency of the PWM/PPM mode, since the wide bandwidths of switching waveforms make resonating out unwanted capacitances somewhat difficult. The situation should improve at lower carrier frequencies. The EER mode has excellent efficiency for most amplifier

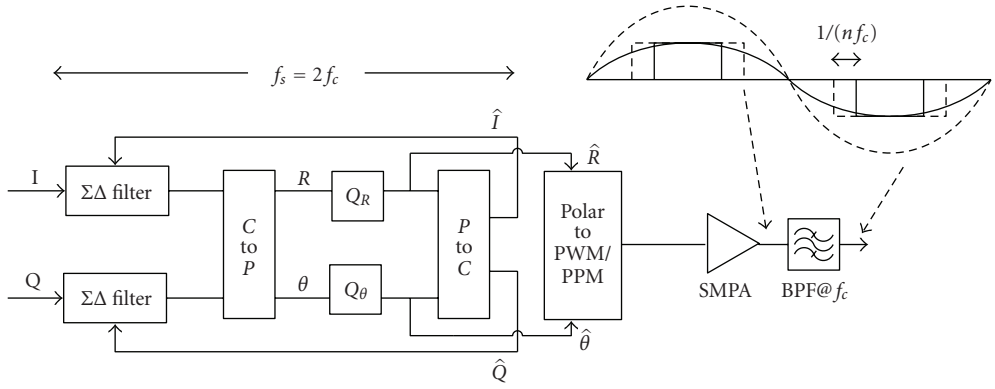

Figure 12: Block diagram of cartesian sigma delta.

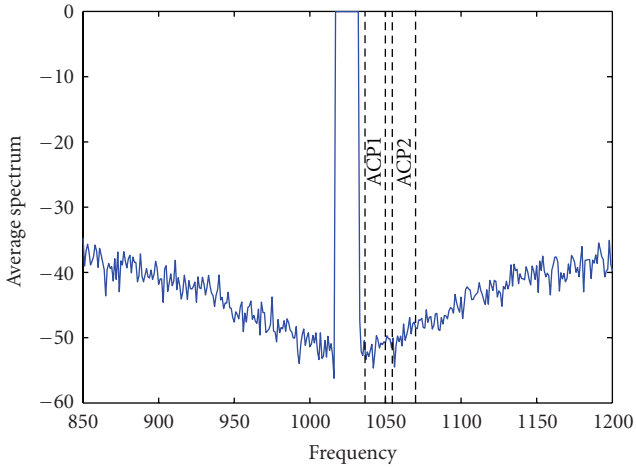

Figure 13: Spectrum plot of Cartesian sigma delta, $n = 16$, $f_c = 1024$ MHz, OFDM channel bandwidth = 20 MHz.

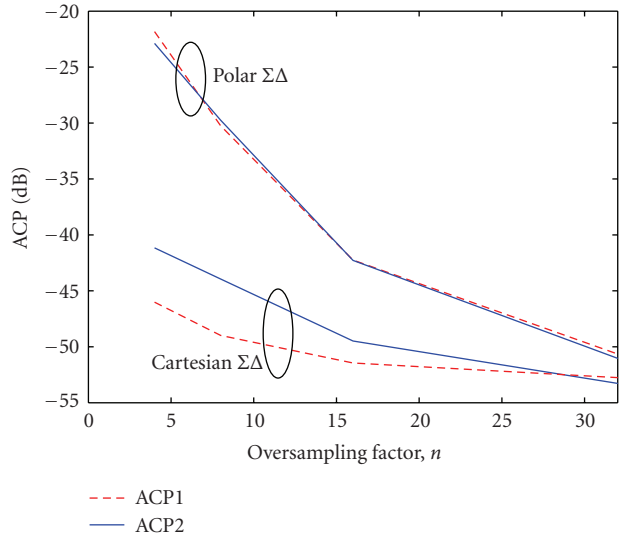

Figure 14: Plot of ACP (dB) against oversampling rate, n. The first and second adjacent channels are shown.

classes, and the amplifier described here is no different. The major limitation of EER is the envelope bandwidth. We have not considered the DC/DC converter in this work, but we have shown that most of the EER efficiency can be conserved if the envelope bandwidth is limited to no less than 0.75 channel bandwidths. The ACI and EVM distortion that this causes in the RF output can be removed by varying the amplitude (in this case using PWM) of the phase modulated input drive signal. Further reduction in the envelope bandwidth requires the PWM waveform to have high efficiency over a greater dynamic range.

The PWM/PPM amplifier drive signal can be directly formed from the I and Q digital baseband signals using ΣΔ techniques to mitigate time quantisation of the pulse edges. The improved performance of the Cartesian filtering in the ΣΔ enables coarser time quantisation of the RF carrier signal. Even so, the digital clock must oversample the RF carrier by a factor of four to meet the WLAN spectral mask and by at least a factor of sixteen to meet the more demanding WCDMA specification. Even though the CREE amplifier is good to 6 GHz [7], it is the digital modulating circuits that limit the maximum carrier frequency.

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