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Research Article

Modified Polar Sigma-Delta Transmitter for Multiradio Applications

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Radio transmitters capable of transforming variable envelope signals into constant envelope signals can be associated with high-efficiency switched mode power amplifiers. One of the techniques providing this conversion is Polar Sigma-Delta ($\Sigma\Delta$) architecture. This approach provides efficient solution for high-dynamic signals, and, moreover, it offers flexibility in a multiradio environment. The overall concept of the polar $\Sigma\Delta$ transmitter is presented here along with novel modifications and improvements. Namely, when recombining the envelope and the phase signals, it is suggested to replace the analog mixing by a digital mixing. The impact of a frequency synthesizer with a switched loop bandwidth and its imperfections on the overall polar $\Sigma\Delta$ architecture is investigated as well. The Mobile WiMAX standard has been chosen for validation due to very high requirements in terms of power dynamics and the variable channel bandwidth. Simulation results are presented in this paper, and advantages and drawbacks of this novel approach are pointed here as well.

1. Introduction

Recent years have seen a considerable development of wireless communication systems such as cellular communications, Personal Area Networks (PANs), Local Area Networks (LANs), and Metropolitan Area Networks (MANs), and they keep evolving at a rapid pace. Coexistence of different wireless standards on the same device is necessary to satisfy all users who expect mobility, ubiquitous connection, and high data rates. At the same time, this coexistence should not penalize the size of the radio device nor reduce the battery life.

Building separate transceivers for individual modes of operation is a straightforward task, and it provides the best performance for each mode, but on the other hand, it significantly penalizes the overall complexity, power consumption, and implementation costs. Therefore, a multi-radio transceiver that combines low power and low costs by sharing reconfigurable components and that is capable of generating any arbitrary waveform becomes the ultimate goal. This concept is known as a multi-radio transceiver.

A multi-radio transmitter should be able to support the most diffused wireless communication standards in the radio band of 800 MHz to 6 GHz and be able to adapt its operating parameters to required specifications [1]. It has to cope with variable signal dynamics, which in turn requires high linearity and low-noise performance of the whole transmission chain. Moreover, a multi-radio transmitter has to support variety of different frequency bands and wide range of different channel bandwidths. Furthermore, a cognitive multi-radio is an evolution of the multi-radio concept that is capable of performing efficient environment spectrum scanning. It can adapt to conditions of the environment and user's needs by choosing the most appropriate communication standard.

The polar $\Sigma\Delta$ transmitter may be used for multi-radio applications when the RF elements of the architecture are designed for the most restrictive parameters of a given communication standard, as suggested in [1].

The overall architecture of the polar ΣΔ transmitter is given in Section 2. Suggested modifications are presented and analysed afterwards. Mobile WiMAX standard and related simulation parameters are introduced in Section 3. Section 4 is focused on a particular design of a frequency synthesizer and on the impact on the proposed polar ΣΔ transmitter. The digital mixing approach and simulation results are presented and summarized in Section 5.

2. Polar ΣΔ Architectures for Multi-Radio Applications

To reach very high data throughputs, advanced spectrum-efficient modulation techniques have been employed in modern wireless communication systems. Unlike modulation techniques used in 2G and preceding wireless systems, most of recent wideband modulation techniques such as the Orthogonal Frequency Division Multiplexing (OFDM) imply high Peak to Average Power Ratio (PAPR) and high degree of RF design complexity. The PAPR may reach up to 29 dB, which is the theoretical maximum in case of the mobile WiMAX standard. This in turn implies stringent linearity requirements on linear Power Amplifiers (PAs) that are typically used in homodyne and heterodyne radio transmitters. However, amplification of variable envelope signals by linear amplifiers results in a significant drop of power efficiency due to the large PAs backoff that is required for distortion-free amplification. A solution to this problem may be offered through linearization techniques [2] or through different signal decomposition techniques [3]. Different architectures based on the signal decomposition principle vary, and they can be classified depending on the way the variable envelope is coded and the way the envelope information is reintroduced to the constant-envelope phase signal (recombination or reconstruction of the variable envelope signal).

Polar architectures decompose the high PAPR signal into two components: a constant envelope phase signal and a variable envelope signal. The complex envelope $z(t)$ of a baseband-modulated signal (QPSK, m-QAM, OFDM, etc.) can be expressed as

$$z(t) = z_I(t) + jz_Q(t). \tag{1}$$

The resulting envelope ρ and both phase signals $\cos(\phi)$ and $\sin(\phi)$ are separated, mathematically:

$$\rho(t) = \sqrt{(z_I(t))^2 + (z_Q(t))^2}\,, \tag{2}$$

$$\cos(\phi) = \frac{z_I(t)}{\rho(t)}, \quad \sin(\phi) = \frac{z_Q(t)}{\rho(t)}\,. \tag{3}$$

The purpose of the decomposition is to amplify the constant envelope signal in a high-efficiency nonlinear switched mode RF PA (that offers theoretically 100% efficiency as the current and the voltage arises at different time intervals) and, moreover, to avoid AM/AM and AM/PM distortions [4, 5].

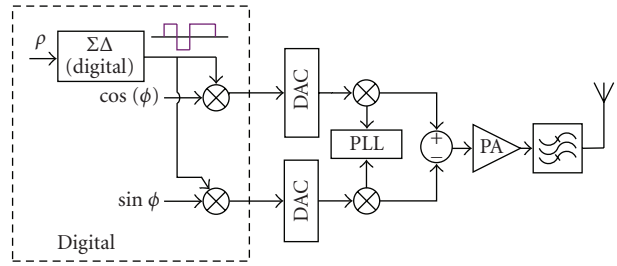


Figure 1: Architecture of a polar ΣΔ transmitter with baseband recombination.

Specific classification of transmitters based on these principles is summarized in [1]. Particularly, two different approaches to the polar ΣΔ transmitter have been introduced in [6, 7].

Polar architecture proposed in [7] modulates the baseband envelope signal ρ by a 1-bit low-pass ΣΔ modulator (having a variable output $\pm a$) and thereby transforms the envelope variant signal into a constant envelope signal. Components of the phase signal ($\cos(\phi)$ and $\sin(\phi)$) have inherently constant envelope nature. The envelope and phase signals are then recombined and RF modulated in an IQ modulator or in a modulated Phase Locked Loop (PLL). Since the resulting recombined signal has a constant envelope, a high-efficiency switched mode amplifier can be used. Amplified signal is then filtered by a band-pass filter to restore the initial shape of the signal (Figure 1).

Another approach proposed in [6] is depicted in Figure 2. This architecture has been optimized in [8] to overcome the noise convolution problem and to improve the in-band Signal to Noise Ratio (SNR) performance. Nevertheless, the proposed improvements use feedback loops, which in turn reduce the maximum bandwidth of the input signal (as the whole feedback systems acts as a low-pass filter).

When comparing these two polar architectures, it is evident that in [7], the restoration of the envelope and the phase is carried out in the baseband, and hence, the synchronization becomes easier compared to the RF polar ΣΔ transmitter [6].

Delay mismatch between the envelope and phase signals is not as severe issue as in the classical Envelope Elimination and Restoration (EER) architecture [1]. However, one of the challenges of this architecture (as any polar architecture) comes out from the conversion from Cartesian to Polar coordinates. This conversion leads to bandwidth expansion and, therefore, to higher requirements on the sampling rate.

In the polar architecture proposed in [7], the output signal of the ΣΔ modulator as well as the $z_I(t)$ and the $z_Q(t)$ signals ($\rho\cos(\phi)$ and $\rho\sin(\phi)$) are digital. Therefore, as shown in Figure 1, two Digital-to-Analog Converters (DACs) need to be employed before the upconversion stage. The sampling frequency of DACs is chosen according to the ΣΔ frequency and it has to be high enough to avoid undesired overlapping of the ΣΔ quantization noise [9]. Communication standards in our multi-radio concept require high ΣΔ frequencies and therefore significant sampling frequency for DACs.

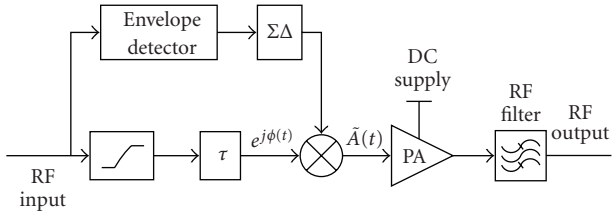


Figure 2: Architecture of a polar ΣΔ transmitter with RF recombination [6].

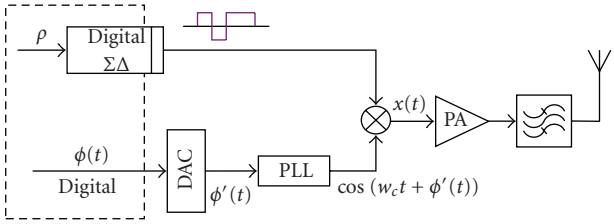


Figure 3: Architecture of the modified polar ΣΔ transmitter.

From this point onward, the polar ΣΔ architecture notation will refer to the architecture proposed in [7].

2.1. Modified Polar ΣΔ Architecture. Instead of decomposing the complex envelope signal into $\rho(t)$, $\sin(\phi)$, and $\cos(\phi)$ as suggested in [7], the modified architecture depicted in Figure 3 separates the envelope and phase signals into $\rho(t)$ and $\phi(t)$ and processes them independently. Digital phase signal is converted to analog and then modulated to the carrier frequency f_c. Finally, the constant envelope signal and the phase signal are recombined. The advantage compared to [7] is that only one DAC is required. Furthermore, DAC frequency requirements can be relaxed. Independent processing of $\rho(t)$ and $\phi(t)$ is also suggested in [6]; however, this approach does not consider issues related to DAC conversion and issues regarding the appropriate choice of DAC and ΣΔ sampling frequencies. The latter issues are analyzed hereafter in detail.

The polar ΣΔ architecture proposed in [7] upconverts the baseband signal to the carrier frequency through an analog IQ modulator. Similarly, the modified ΣΔ architecture we propose here employs an analog multiplier to recombine the envelope and phase signals. The next section suggests generating a digital carrier and replacing the analog mixer by a digital mixer.

2.2. Polar ΣΔ Architecture with Digital Mixing. Figure 4 presents a scheme of the digital mixing polar ΣΔ architecture. In this case, an All Digital PLL (ADPLL) generates the carrier frequency. The digital mixing can be assured by an AND gate as suggested in [10]. Compared to the architectures proposed in [6, 7], our approach to the ΣΔ architecture offers more flexibility due to the nature of the digital signal processing, and, moreover, it offers better IC integration.

Synchronization between the envelope and phase signals is a critical point in this particular polar architecture. To overcome this problem, it is suggested in this third approach to use a common reference frequency for the digital PLL and for the ΣΔ modulator.

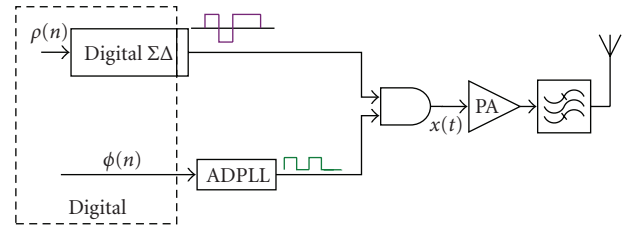


Figure 4: Architecture of the polar ΣΔ transmitter with digital mixing.

Multiplication of the ΣΔ modulated envelope and the modulated phase in the time domain corresponds to a convolution in the frequency domain. The output is then centred at 0, $3f_0$, $5f_0$, and so forth, and the quantization noise introduced by the ΣΔ modulator is symmetrical around the carrier.

3. Simulations of the Modified Polar ΣΔ Architecture: Mobile WiMAX Validation

Mobile WiMAX is a very flexible wireless communication standard, which offers a choice among a range of different channel bandwidths that vary depending on the expected throughput and the allocated radio frequency band. The channel bandwidth may vary from 1.75 MHz to 20 MHz.

The multi-radio architecture must support any of the configurations defined by the standard. This communication standard has been chosen in our simulations due to high envelope dynamics, relatively high channel bandwidths and very high requirements for the frequency synthesizer (in terms of integrated phase noise, frequency range, and settling time). The Mobile WiMAX operates at higher frequencies than any other cellular systems, and, hence, this fact draws the attention to the influence of the carrier frequency on the performance of the polar ΣΔ architecture.

3.1. Mobile WiMAX Technology. Mobile WiMAX standard supports mapping according to the QPSK, 16-QAM, or 64 QAM constellation schemes using the Orthogonal Frequency Division Multiplexing (OFDM) modulation. OFDMA air interface is based on the OFDM modulation and corresponds to the nonline of sight operation in licensed frequency bands below 11 GHz. The FFT size can vary between 2048, 1024, 512, and 128 [11]. Following parameters characterise the OFDMA: channel bandwidth BW, number of used subcarriers N_{used} and DC subcarriers, sampling factor n, and the cyclic prefix to useful time ratio G [11]. Channel bandwidths and the number of subcarriers are chosen depending on the selected frequency band, channel conditions, capacity, and the expected throughput. The factor n depends on the BW. Supported values for the G are 1/32, 1/16, 1/8, and 1/4. Certification profiles published by the WiMAX Forum

Table 1: Mobile WiMAX certification profiles [12, 14].

Frequency band (MHz)	Channel BW (MHz)	FFT size	Settling time (μs)	Phase jitter (°rms)
2300–2400	5	512		
	8.75, 10	1024		
2305–2320	3.5, 5	512		
2345–2360	10	1024		
2496–2690	5	512	<50	<1
	10	1024		
3300–3400	5	512		
	7,10	1024		
3400–3800	5	512		
3400–3600				
3600–3800	7,10	1024		

specify the frequency range, channel bandwidth, and the FFT size [12]. All these profiles use the TDD duplexing mode.

3.2. Simulation Parameters. Following simulations have been conducted using Agilent Advanced Design Software (ADS) and the Matlab simulation tool.

Simulation parameters have been chosen according to the WiMAX Forum certification profiles (Table 1) as follows: carrier frequency = 3.7 GHz, BW = 10 MHz, FFT size 1024, $n = 28/25$, and $G = 1/32$ (throughput privileged) [12]. Raw symbol rate is calculated as specified by [11] using the selected parameters and the 64-QAM modulation scheme (this configuration has been selected to observe the highest PAPR). It is necessary to choose enough samples per symbol in order to respect the emission power mask, which is defined in Europe by [13]. Moreover, number of samples also determines the ΣΔ frequency (symbol rate/number of samples).

The ΣΔ modulator has been synthesized using the Matlab Delta-Sigma Toolbox [15]. A model of a 1-bit Σ △ is shown in Figure 5. The output signal $V(z)$ is given by

$$V(z) = \frac{H(z)}{H(z)+1}U(z) + \frac{1}{H(z)+1}E(z), \tag{4}$$

where E(z) is the quantization noise. The first term of (4) is the Signal Transfer Function (STF), and it corresponds to a low-pass filter. The second term represents the Noise Transfer Function (NTF), and it corresponds to a high-pass filter. NTF can be synthesized using the Matlab toolbox from the following arguments: the order of the NTF, the out-of-band gain of the noise transfer function, the centre frequency of the modulator, and the Oversampling Ratio (OSR). The modulator order is proportionally related to noise-shaping performance and SNR improvement, but on the other hand, low-order ΣΔ modulators are less sensitive to limit cycles, easier to implement, and offer higher stability [15].

A second-order modulator has been chosen for simulations. Since Lee's rule states that a gain minor to 2 yields a stable modulator with a binary quantizer [15], the out-of-band gain has been set to 1.9. Finally, due to the low-pass nature of the modulator, the centre frequency has been set to 0.

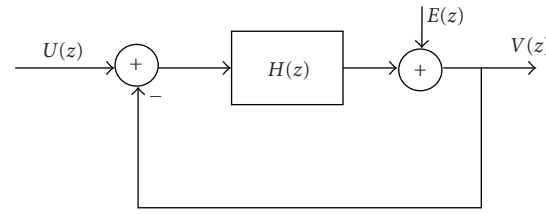


Figure 5: Model of a 1-bit ΣΔ modulator.

The OSR is related to the ΣΔ modulator sampling frequency $f_{\Sigma\Delta}$ and to the input signal bandwidth f_B as follows:

$$\mathrm{OSR} = \frac{f_{\Sigma\Delta}}{2f_B}. \tag{5}$$

The oversampling effect moves the quantization noise toward higher frequencies, which in turn improves the in-band SNR performance. As a result, antialiasing requirements can be relaxed.

However, by increasing the OSR value, we compromise on the ΣΔ feasibility (need for higher sampling frequency), and it also increases the power consumption. As higher ΣΔ frequency leads to higher implementation complexity and higher costs and power consumption [15], the choice of the ΣΔ modulator frequency $f_{\Sigma\Delta}$ becomes a crucial point, and it is directly related to the transmitter carrier frequency f_c.

Power spectrum of the baseband ΣΔ-coded envelope signal is replicated at the multiples of the sampling frequency $f_{\Sigma\Delta}$. The transposition of the coded signal on the carrier frequency corresponds in the frequency domain to a convolution with the carrier. During this modulation process, the out-of-band quantization noise is modulated as well and reaches the maximum value at every unpaired multiples of the $f_{\Sigma\Delta}/2$ ($f_{\Sigma\Delta}/2$, $3f_{\Sigma\Delta}/2$, $5f_{\Sigma\Delta}/2$, etc.) while the minimum value of the quantization noise appears at every multiple of $f_{\Sigma\Delta}$ ($f_{\Sigma\Delta}$, $2f_{\Sigma\Delta}$, $3f_{\Sigma\Delta}$, etc.). This frequency transposition is depicted in Figure 6.

If the $f_{\Sigma\Delta}$ is superior to $2f_c$, the signal in the useful bandwidth will be disturbed by the quantification noise at the multiples of the $f_{\Sigma\Delta}$. Hence, to avoid the quantification noise overlapping that may lead to a signal to noise ratio degradation in the useful signal bandwidth, the following condition must be respected [16]:

$$f_{\Sigma\Delta} \leq 2f_c. \tag{6}$$

Moreover, as the quantification noise reaches the minimum at multiples of $f_{\Sigma\Delta}$, it is convenient to fix

$$f_{\Sigma\Delta} = \frac{2f_c}{m}, \tag{7}$$

where m is a positive integer number.

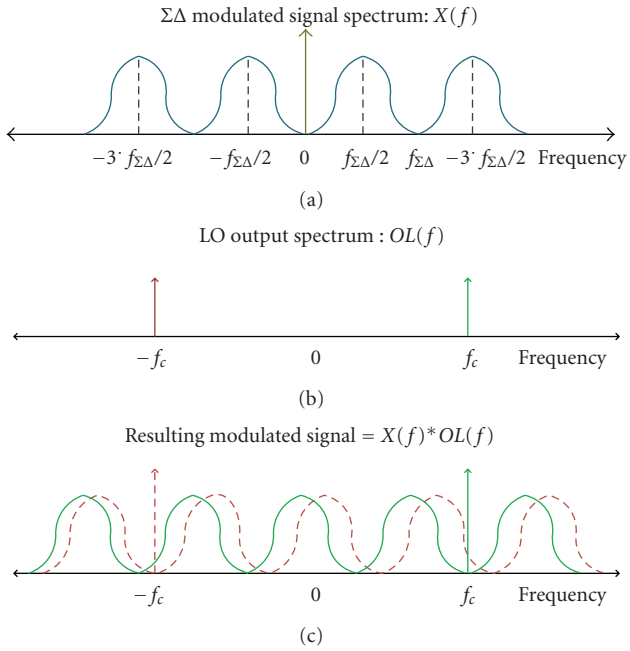


Figure 6: Modulation of the envelope ΣΔ coded signal.

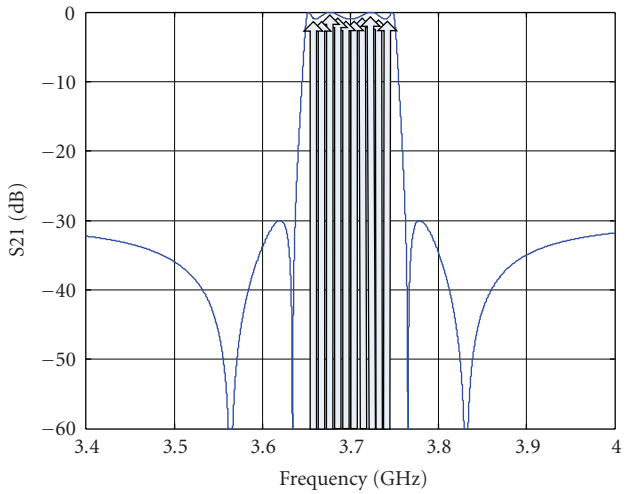


Figure 7: Allocated frequency band and individual channels.

This choice also simplifies the circuit implementation and the synchronization between the envelope and phase, because the same reference frequency can be used for both, the PLL and the ΣΔ modulator.

In this paper, the factor m has been set to 2, and the carrier frequency is 3.7 GHz. Therefore, the same frequency has been chosen for the ΣΔ modulator.

From Table 1, it can be seen that the WiMAX frequency band from 3.4 to 3.8 GHz is divided into two bands of 200 MHz. In order to analyze the higher carrier frequency of 3.7 GHz, the second band has been chosen for simulations.

A 100-MHz bandwidth is considered at the output of the transmitter, and, therefore, any 10 MHz channel within this band can be transmitted (Figure 7).

The bandwidth of the ΣΔ modulator f_B is then fixed to 100 MHz. From (5), the OSR value used to synthesize the ΣΔ modulator NTF is then 18.

Instead of a feed-forward structure, a feedback ΣΔ structure has been selected because of its flat response, lower risk of overvoltage, and better stability [15].

4. Frequency Synthesizer

In the previous sections, an ideal frequency synthesizer has been considered. This section investigates the impact of a real frequency synthesizer on the performance of the previously presented modified polar ΣΔ architectures.

A frequency synthesizer generates a local frequency that is mixed with the incoming RF signal to create a lower frequency signal that can be digitized and processed in the baseband IC. A frequency synthesizer has to provide all necessary frequencies for the down-and upconversion with proper channel spacing that corresponds to the channel bandwidth or to the frequency raster. Frequency switching has to be performed agilely, with respect to settling time requirements of the standard. Moreover, the local frequency synthesizer has to fulfil the tightest signal purity requirements that can be expressed in terms of the integrated phase noise and the spurious output. These requirements given by the Mobile WiMAX standard are summarized in Table 1 [12, 17].

It can be seen that the most critical requirements are given in terms of the integrated phase noise and the settling time. The integrated phase noise is to be less than 1° rms within an integration bandwidth of 1/20 of the tone spacing (modulated carrier spacing) to 1/2 of the channel bandwidth [17]. Thus for smaller channel bandwidths, the integration of the phase noise can start from as low as a few hundred Hertz, which results in worse phase jitter performance. Moreover, the frequency synthesizer has to settle within less than 50 μs [18]. The minimum required frequency resolution is derived from the required channel raster, which is 250 kHz.

4.1. Frequency Synthesizer Architecture. Due to very high requirements given by the Mobile WiMAX standard, a PLL-based fractional-N frequency synthesizer has been chosen. This PLL architecture can achieve very small frequency resolution equal to the fractional portion of the reference frequency and hence improve the in-band phase noise performance. Frequency synthesizer presented in this paper employs a switched loop bandwidth topology that significantly improves the settling time performance [19, 20]. A simplified linear model of the synthesizer is depicted in Figure 8.

This model includes a tristate PFD (Phase Frequency Detector) that produces output *up* and *down* signals proportional to the phase and frequency difference between the reference and the feedback signal. The PFD employs two positive edge-triggered resetable FF (Flip-Flops) to detect the phase and frequency difference and one AND gate to monitor the *up* and *down* signals. The upper FF is clocked by f_{ref}, the lower by f_{div}. Signals *up* and *down* are used to switch current

sources in the Charge Pump (CP). These CP current pulses change the voltage drop on the loop impedance and tune the VCO with tuning gain of 125 MHz/V and tuning range of 3.4–3.88 GHz.

The basic idea behind the switched loop bandwidth topology is to use a larger loop bandwidth during the frequency transition and, then, after a certain programmable period, to shift the loop bandwidth to the normal narrow value. To understand the switching principle, let us have a look at the PLL control theory and the PLL linearized model. The effect of a closed feedback loop on the input reference signal φ_{in} can be described by the closed loop transfer function $T(s)$ as

$$T(s) = \frac{\phi_{\text{out}}(s)}{\phi_{\text{in}}(s)} = \frac{G(s)}{1 + G(s)H}, \tag{8}$$

where $G(s)$ represents the open loop transfer function and H corresponds to the division factor $1/N$.

Now, let us define the CP/PFD gain as K_d that equals $I_{cp}/2\pi$, the VCO gain K_{vco} and the loop filter trans-impedance $F(s)$. Hence, (8) turns into

$$T(s) = \frac{K_d K_{vco} F(s)/s}{1 + K_d K_{vco} F(s)/Ns}. \tag{9}$$

The transimpedance of the second-order loop filter depicted in Figure 9 is given by

$$F(s) = \frac{1 + sC_2R_2}{s(C_1+C_2)(1 + sC_1C_2R_2/C_1+C_2)}. \tag{10}$$

The angular open loop crossover frequency and the phase margin (hereafter referred to as ω_c and θ_c, resp.) are defined at the point where the open loop gain reaches unity. This can be expressed as $\|G(s)H\| = 1$ (0 dB), where $G(s)H$ is given by

$$G(s)H = \frac{K_d K_{vco} F(s)}{sN} = \frac{I_{cp} K_{vco} F(s)}{2\pi sN}. \tag{11}$$

By defining time constants T_2 and T_1 of zero and the pole in the second order loop filter transfer function, respectively, as $T_2 = C_2R_2$, $T_1 = C_1C_2R_2/(C_1 + C_2)$, the equation can be written as

$$|G(s)H|_{s=j\omega} = -\frac{I_{CP}K_{VCO}}{2\pi\omega_c{}^2N} \cdot \frac{1 + j\omega_c T_2}{1 + j\omega_c T_1} \cdot \frac{1}{C_1 + C_2}, \tag{12}$$

and then, the open loop phase margin θ_c reads

$$\theta_c[\text{rad}] = \pi + \arctan(\omega_c T_2) - \arctan(\omega_c T_1). \tag{13}$$

Let us consider a situation, where the crossover frequency is increased by factor α in order to increase loop bandwidth and hence decrease the settling time. This adjustment is applied only during the frequency transition. To ensure the loop stability at $\alpha \cdot \omega_c$, the phase margin defined in (13) has to remain constant. This can be done by means of reducing the value of T_2 and T_1 by the factor α with help of a parallel resistor R_s as displayed in Figure 9.

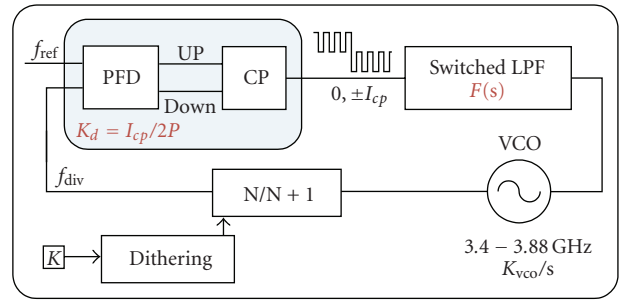


Figure 8: Linear model of a fractional-N charge pump synthesizer.

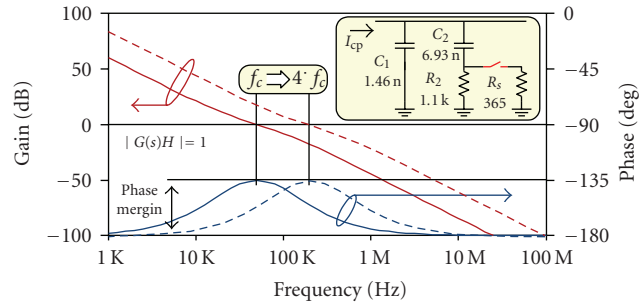
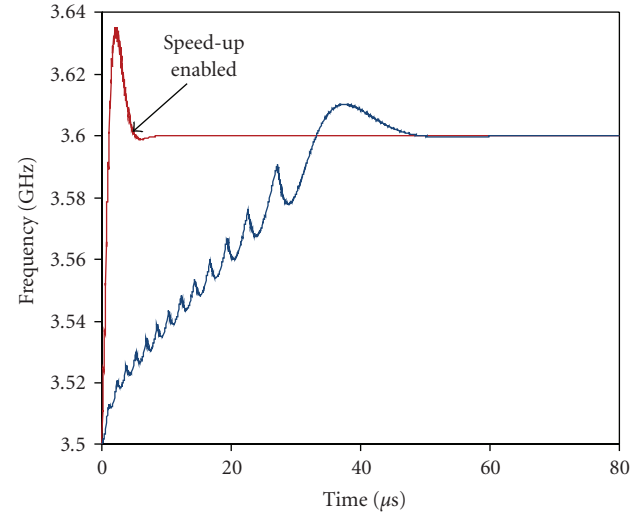


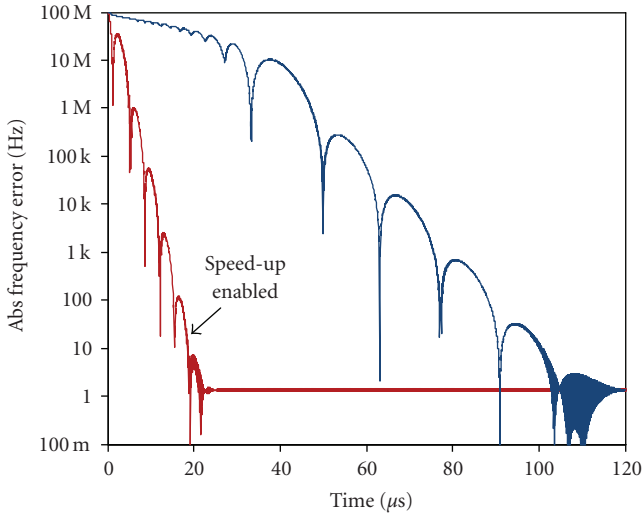
Figure 9: Open loop gain for both PLL loop filter configurations. The loop stability is unaffected (phase margin remains constant= 44.7°).

Moreover, the product of all elements in (12) has to be increased by factor of α^2 as the angular frequency ω_c in (12) is in the power of two. This can be done by means of increasing the charge pump current I_{cp} by factor α^2.

The speedup mode in our architecture is achieved when the CP current is increased by a factor of 16 ($I_{cp} \rightarrow 16 \cdot I_{cp}$) while reducing the dumping resistance by factor of 4 ($R_2 \rightarrow R_2/4$). Hence the PLL open-loop cross-zero frequency and the zero and pole frequency ($1/R_2C_2$ and $1/[R_2C_1C_2/(C_1 + C_2)]$) are all increased by a factor of 4. The loop stability remains unaffected. The dumping resistance is reduced by factor of 4 by using an extra parallel resistor R_s. This resistor is chosen such that the parallel combination of the dumping resistor R_2 and the resistor R_s equals to 1/4 of the original value of the dumping resistor R_2. To determine the optimal moment to shift the loop bandwidth to the normal (narrow) value, the following simulation has been carried out. Settling time has been monitored while changing the time spent in the wideband mode during the frequency transition. This time period has been calculated by the reference counter in terms of reference frequency cycles. One reference cycle equals to 31.25 ns ($1/32 \cdot 10^6$). It has been found that the major settling time improvement due to the speedup mode occurs approximately within the first 425 reference cycles, which corresponds to 13.3 μs. From this moment onward, the settling time remains roughly constant, and hence it is no more beneficial to stay in the wideband mode. This time period has been considered as the optimal time to switch the loop bandwidth to the normal value. Figure 10 shows the



(a)



(b)

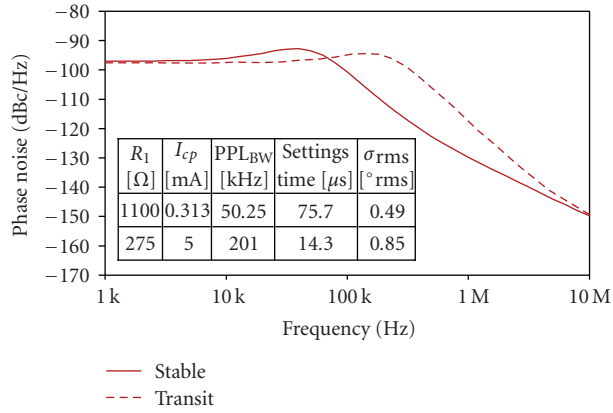
Figure 10: Transient responses of the PLL for two cases: speedup mode enabled/disabled (red/blue line, resp.). Plot (b) shows the absolute frequency error relative to the settling frequency 3.6 GHz.

corresponding transient response of the PLL synthesizer that hops from 3.5 to 3.6 GHz. Moreover, the absolute frequency error in reference to 3.6 GHz is depicted in Figure 10, plot b).

Notice that the PLL can settle with the maximal accuracy of 1 Hz. This error is caused by the leakage current that flows from the CP to the loop filter and causes undesired voltage drop that tunes the VCO. In this particular simulation, the 1-Hz uncertainty was caused by 1 nA leakage current. In addition to that, the leakage current contributes to reference and fractional spurs.

Resulting phase noise performance of this synthesizer at the carrier frequency 3.7 GHz for both loop filter configurations is depicted in Figure 11 along with corresponding adjustment of loop filter parameters.

The integrated phase noise σ_{rms} has been calculated from 488 Hz to 5 MHz. This integration bandwidth corresponds



R_1 [Ω]	I_{cp} [mA]	PPL_{BW} [kHz]	Settings time [μs]	σrms [° rms]
1100	0.313	50.25	75.7	0.49
275	5	201	14.3	0.85

Figure 11: Phase noise performance at 3.59 GHz. Dashed line corresponds to the noise behaviour at the PLL output during the frequency transition (wideband mode).

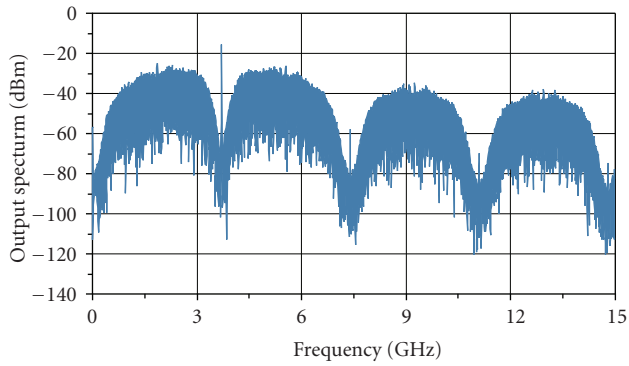


Figure 12: Signal spectrum of the modified polar ΣΔ architecture ($f_{\Sigma\Delta}$ = 3.7 GHz).

to the channel bandwidth 10 MHz and FFT size 1024. It is evident that the integrated phase noise has risen in the transient mode due to the PLL bandwidth enlargement, but on the other hand, the settling time has dropped from 75.7 μs to 14.4 μs. Moreover, as the wideband mode is employed only during the frequency transition, which is very short, the higher phase noise does not affect the performance of the synthesizer. This performance of the frequency synthesizer has been considered during the co-simulations of the modified polar ΣΔ architectures and it has been observed that the overall performance of the transmitter in terms of the EVM has not been deteriorated (the EVM = 1.4% in both cases).

5. Simulation Results of the Digital Mixing Architecture

Figure 12 presents the output spectrum of the modified polar ΣΔ architecture as described in the Section 2.1.

Figure 13 presents the output spectrum of the digital mixing polar ΣΔ architecture described in the Section 2.2. Simulation parameters are summarized in Sections 3 and 4.

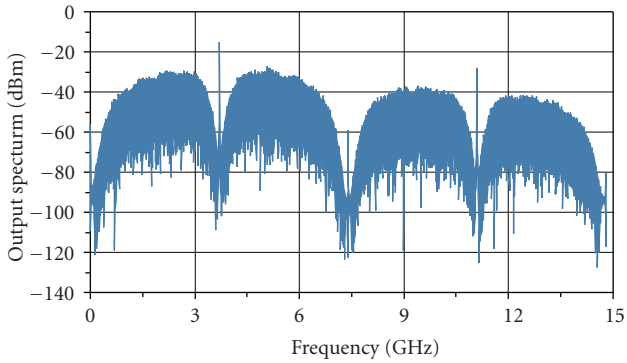


Figure 13: Signal spectrum of the polar ΣΔ architecture with digital mixing ($f_{\Sigma\Delta} = 3.7$ GHz).

Table 2: Maximum possible oversampling ratio for the most diffused mobile communication standards.

Standard	Frequency [MHz]	f_c [MHz]	Band [MHz]	Channel BW [MHz]	OSR
GSM 900	890–915	902.5	25	0.2	18 / 2256
DCS 1800	1710–1785	1747.5	75	0.2	11 / 4368
UMTS/ WCDMA	1920–1980	1950	60	5	16 / 195
UMTS	1900–1920	1910	20 /	5	47 / 191
	2010–2025	2012.5	15		67 / 201
802.11 b/g	2400–2483.5	2441.75	83.5	11	14 / 110
802.11a	5150–5350	5250	200	20	13 / 131
	2300–2400	2350	100		11 / 117
Mobile WiMAX (802.16e)	2496 – 2690	2593	194		6 / 129
	3300 – 3400	3350	100	10	16 / 167
	3400 – 3600	3500	200		8 / 175
	3600 – 3800	3700	200		9 / 185

It can be seen that a single frequency component (that was not present in the analog mixing ΣΔ architecture) appears at $3f_c$ (11.1 GHz, see Figure 13). The spectrum replication, which is common in the digital mixing, can lead to noise overlapping and may deteriorate the SNR in the transmission bandwidth. Therefore, to assure the overlapping-free transmission, the ΣΔ modulator frequency has to be chosen according to (6) and (7). Unfortunately, these conditions are not always easy to respect in a multi-radio system, and there is always a tradeoff between the high oversampling ratio and the feasibility and implementation of the ΣΔ modulator. Certain communication standards may require a very high oversampling ratio of the ΣΔ modulator even though their transmitting frequency is not relatively high. This fact points out the importance of the correct evaluation of the relation between the signal bandwidth and the carrier frequency for each communication standard [21].

Let us consider again the WiMAX case. Even though the bandwidth chosen to calculate the OSR is 100 MHz, the real occupied bandwidth during the transmission will be only 10 MHz (i.e., the channel bandwidth). However, the choice of using the allocated bandwidth for the OSR calculation instead of the channel bandwidth is justified, because the quantification noise is minimised in the whole frequency band. This assumption in turn alleviates requirements for the output RF filter.

Another reason for choosing a wider bandwidth for the ΣΔ modulator is to avoid the convolution noise that appears during the recombination of the envelope and phase signals. The frequency band occupied by the phase signal is wider than the frequency band of the input signal, which implies that during the phase and envelope recombination (convolution in the frequency domain) one part of the envelope quantification noise can be introduced in the useful signal bandwidth and affect the final SNR performance.

Table 2 presents the maximum OSR that can be reached for given mobile communications standards. It is calculated from (5). There are two values; the first value is calculated according to the complete allocated bandwidth, and the second value is calculated according to the channel bandwidth.

6. Conclusion

In this paper, we have presented a polar ΣΔ transmitter as a suitable candidate for multi-radio applications, and, moreover, we have proposed novel modifications and improvements to this architecture. Viability of using the proposed derivative architectures for multi-radio applications has been studied and validated on the Mobile WiMAX standard. It has been shown that proposed modifications can significantly decrease the overall circuit complexity compared to the previously proposed polar architectures. The latter modifications consider namely direct PLL modulation and digital mixing when recombining the envelope signal with the phase signal. Moreover, synchronization issues have been addressed as well. We have demonstrated that certain conditions related to the frequency of the ΣΔ modulator and the signal bandwidth need to be fulfilled to assure accurate operation and to maximize the SNR. It has also been shown that to achieve high oversampling ratio, polar architectures require high ΣΔ frequency. This has been demonstrated on the Mobile WiMAX standard and theoretical values for the maximum oversampling ratios for other communications standards have been calculated as well.

To approach to more realistic analyses, we didn't focus only on the polar architecture itself, but we have also investigated the impact of a real frequency synthesizer with its inherent imperfections (such as phase noise and spurious signals) on the performance of the overall architecture. The proposed synthesizer employs switched loop bandwidth topology, which allows operating in a wideband mode during the frequency transition and hence achieves high switching speed. A narrowband mode is employed in the stable state to achieve superior phase noise and spurious performance. The degradation of the EVM due to the synthesizer phase noise during the reciprocal mixing has been investigated as well, and it has been shown that the combination of the proposed

synthesizer and the polar architecture can fulfil requirements imposed by the Mobile WiMAX standard.

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