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Parametric Conversion Using Custom MOS Varactors

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The possible role of customized MOS varactors in amplification, mixing, and frequency control of future millimeter wave CMOS RFICs is outlined. First, the parametric conversion concept is revisited and discussed in terms of modern RF communications systems. Second, the modeling, design, and optimization of MOS varactors are reconsidered in the context of their central role in parametric circuits. Third, a balanced varactor structure is proposed for robust oscillator frequency control in the presence of large extrinsic noise expected in tightly integrated wireless communicators. Main points include the proposal of a subharmonic pumping scheme based on the MOS varactor, a nonequilibrium elastance-voltage model, optimal varactor layout suggestions, custom 0.13 μm-CMOS varactor design and measurement, device-level balanced varactor simulations, and parametric circuit evaluation based on measured device characteristics.

1. INTRODUCTION

Variable capacitors can play a very rich role in radio-frequency (RF) transceivers. In this paper we examine their use in two key front-end functions: amplification and frequency control. Parametric amplification, a relatively uncommon technique, is promoted in this paper. Improvements to this method are proposed by the incorporation of customized MOS varactors in place of the traditional junction varactor. Also, we discuss modifications to the MOS varactor in the context of its traditional role as a frequency control element. Anticipating a growing problem with interference between IC elements sharing one substrate, a four-terminal differential structure intended to desensitize voltage-controlled oscillators (VCOs) to large extrinsic noise variations is described.

The paper is organized as follows. First a narrow outline of the history and status of parametric amplification is given in Section 2. A more detailed discussion of parametric circuit operation, improvements, and possible incorporation in a front-end transceiver is discussed in Section 3. Since the varactor constitutes the heart of parametric systems, Section 4 outlines the key integrated varactor structures, compares them based on two key merit figures, and introduces potential device-level augmentations. In Section 5 we return to parametric circuits and, with the results of Section 4, estimate the performance possibilities for an integrated setting. Frequency control, the second key topic of this report, is discussed in Section 6. This is approached from the device level, where the advantage and limitations of employing a modified common-mode rejection varactor structure in a voltage-controlled oscillator (VCO) are discussed.

2. PARAMETRIC CONVERSION: HISTORICAL REMARKS

Parametric circuits closely tie frequency conversion to amplification and therefore can seamlessly account for the mixing function of front ends as well. We broadly refer to them as parametric converters in this work. They are primarily known for their low-noise behavior and ability to operate at high frequencies.

As implied by its name, parametric conversion involves the modulation of a system's parameters as in the damped oscillatory equation below:

$$\ddot{x} + \gamma\dot{x} + \omega_0^2[1 + p(t)]x = 0. \tag{1}$$

Given a pumping disturbance at twice the oscillator's natural frequency,

$$p(t) = A_p \sin(2\omega_0 t), \tag{2}$$

A subharmonic (relative to the pump) response

$$x(t) = A_s e^{\alpha t} \sin \omega_0 t \tag{3}$$

can be solicited where α ranges between positive and negative values depending on the oscillator damping and the strength of the pumping signal. It is commonly acknowledged that such sustained parametric oscillations were first observed by Michael Faraday. In 1831 he reported the rise of subharmonic oscillation as part of experiments on acoustically pumped Chladni plates [1]. In 1957, following suggestions by Suhl [2] and Weiss [3], he reported the realization of an experimental solid-state microwave amplifier exploiting the parametric principle. Notable among a large number of intermediate contributions is Hartley's work on electromechanical parametric amplifiers [4, 5] and Barrow's fully active parametric vacuum tube implementation [6]. This space has been a subject of interest in the MEMS arena for low-frequency, precision sensing applications such as atomic force microscopy [7, 8] where the low-noise properties of parametric systems are of particular benefit. However, the use of parametric amplification in terrestrial communication systems is extremely rare. Recently, a discrete time parametric circuit in a 0.25 μm-CMOS technology was reported [9]. The circuit took particular advantage of the three-terminal inversion mode MOS varactor, but focused on low-frequency applications in the 100 kHz range.

The absence of parametric converters from the communications mainstream is mainly due to the superior utility of transistor-based circuits for "low-" frequency commercial applications. Since the performance of parametric circuits is less dependent on the lateral dimensions (and hence delay) of their components, a key advantage of this approach is its ability to operate at higher frequencies early in the technology life cycle. However, improvements in transistor technology steadily encroached on the high-frequency reserve of parametric circuits thus marginalizing this advantage. Since more remote regions of the spectrum were better accommodated by maser and laser amplifiers, a loss of interest in the parametric circuit approach followed.

Today, as personal commercial communications applications migrate to more exotic frequency domains, a niche for the parametric circuit may resurface. This may especially be the case for low-profile millimeter wave electronics intended for dense sensor or distributed network applications. Size and power constraints exclude many of today's molecular amplifiers (although integration progress has been substantial [10]) from consideration while performance, power, and approaching physical limits have relegated millimeter wave applications to the domain of expensive IC technologies.

3. PARAMETRIC CONVERSION: TECHNICAL REMARKS

Conventional electronic transistor amplifiers operate by using a small signal to modulate the resistance of a switch that, in turn, mediates the coupling between a large DC supply and a load. Amplification is achieved because the coupling is proportional to the small input signal and is efficient because, ideally, the supply does not influence the modulated resistance. Alternatively, parametric amplifiers utilize a nonlinear reactance (in this paper we consider only capacitive reactances) through which an AC supply "energizes" a small signal. More specifically, a small signal deposits charge on a capacitor. An AC "pump" increases the potential energy of this charge by increasing the capacitance, the pumped charge is then siphoned off to a load.

Immediately it is apparent that by foregoing resistive coupling such an amplification principle sidesteps, at least in part, thermal fluctuations and holds inherent noise behavior advantages. A handy "existance theorem" of sorts for parametric converters is available in the form of the Manley-Rowe relations [11]

$$\sum_{m=0}^{\infty}\sum_{n=-\infty}^{\infty}\frac{mP_{m,n}}{mf_s+nf_p}=0,$$
$$\sum_{n=0}^{\infty}\sum_{m=-\infty}^{\infty}\frac{nP_{m,n}}{mf_s+nf_p}=0. \tag{4}$$

The ideal circuit used to derive the Manley-Rowe relations is shown in Figure 1. These relations constrain the power, $P_{m,n}$, absorbed by a nonlinear capacitor at frequencies $mf_s + nf_p$ that is driven by two sources operating at frequencies f_s (the signal source) and f_p (the pump source). The relations are fundamental in that they are based on the principle of energy conservation (zero total average power flowing into the capacitor) and are independent of the capacitance-voltage (CV) characteristics (aside from assuming no hysteresis in the voltage); the relations are limited in that they do not account for losses in the varactor which have a substantial impact on practical implementations.

The raw circuit performance encapsulated by Manley-Rowe relations needs to be constrained in order to realize practical functions like upconversion (signal at f_s amplified and mixed to higher frequencies) or downconversion (signal at f_s amplified and mixed to lower frequencies) or simply straight amplifiers (signal at f_s amplified at f_s). The common way of doing this is to encase the capacitance in a multimode cavity. From a lumped circuit perspective, this means connecting the capacitance to some assembly of resonators.

3.1. Upper-sideband upconverter

We imagine the nonlinear capacitor locked in a resonant configuration that allows power to flow only at frequencies f_s, f_p, and $f_u = f_s + f_p$. For this scenario equation (4) is simplified to

$$\frac{P_{1,0}}{f_s}+\frac{P_{1,1}}{f_s+f_p}=\frac{P_s}{f_s}+\frac{P_u}{f_u}=0, \tag{5}$$

$$\frac{P_{0,1}}{f_p}+\frac{P_{1,1}}{f_s+f_p}=\frac{P_p}{f_p}+\frac{P_u}{f_u}=0. \tag{6}$$

As stated earlier the pump is our energy source in this circuit, it is responsible for a positive power flow, P_p, into the capacitor. According to (6) this means that the power, P_u, at f_u must be negative, hence flowing out of the capacitor and available

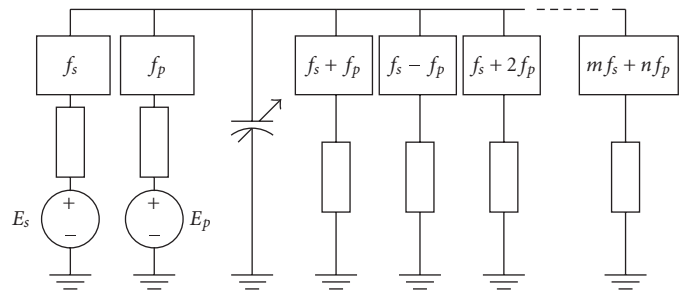


Figure 1: The ideal parametric converter used to derive the Manley-Rowe relations. Ideal impedance filters allow only a single tone to flow through any one branch.

to a load. From (5) the circuit has the operating power gain

$$G_{\text{up}} = \frac{P_u}{P_s} = \frac{f_u}{f_s}. \tag{7}$$

A more physical description of USBUC operation may shed more light on its behavior. The potential energy of the charge that a small signal deposits on a capacitor can be increased by separating that charge. Work is needed to do this and this work is periodically supplied from a pump circuit. Under this condition, when a load extracts this charge from the capacitor, it will have access to higher energy carriers. Gain is achieved. However, the work used to energize the mediating capacitor increases the energy needed by the input signal to charge it again. Thus, the circuit is naturally at an advantage when pumping and energy extraction are done quickly compared to the dynamics of the signal input (i.e., when the capacitor signal is oversampled).

Thus the higher the output frequency (hence pump), the greater the circuit gain. This configuration, the upper-sideband upconverter (USBUC), is well suited for high-frequency transmission. For instance, under ideal conditions, converting a 6 MHz signal to a 60 GHz carrier promises a 40 dB operating power gain making the circuit more attractive for millimeter wave applications. Note that, under the ideal described by (5) and (6) (i.e., lossless varactor and perfect resonator), the gain is completely independent of the pumping power. Analysis and simulations of the impact wrought by varactor losses on circuit gain are presented in Section 5. Of course the maximum available output power is limited by the size of the input and pump signals. For a small input signal and $f_u \gg f_s$ we have a maximum output power of approximately $P_p/2$ hence an efficiency of 50%. As f_s increases the efficiency improves, but the gain drops.

Accounting for losses in the surrounding filter (cavity) network by itself does not directly influence the ideal gain prediction. Rather, as highlighted by Rowe [12], the bandwidth of the converter is compromised. Assuming that the pump's action on the nonlinear varactor introduces a time-varying incremental capacitance between the USBUC's f_s and f_u ports of

$$C_{\text{pump}}(t) = \sum_{n=-\infty}^{\infty} C_n e^{j2\pi n f_p t} \tag{8}$$

the bandwidth to signal-frequency ratio (γ_{up}/f_s) becomes [12]

$$\frac{\gamma_{\text{up}}}{f_s} = \frac{C_1}{C_0}\sqrt{2\frac{f_u}{f_s}}. \tag{9}$$

Returning to the previous example, to accommodate a signal of 10 MHz bandwidth converted from a 6 MHz to a 60 GHz center frequency requires a C_1/C_0 ratio of less than 1/80. This bodes extremely well for the pump. For a well-designed MOS varactor it is not unreasonable to expect a 50% variation around C_0, that is, assuming the common empirical MOS model we expect

$$C_{\text{MOS}} = C_0 + \frac{C_0}{2}\tanh\left(\frac{3}{2}v_{\text{pump}}\right) \approx C_0 + \frac{3C_0}{4}v_{\text{pump}}, \tag{10}$$

where the latter approximation is based on the assumption of a small pump voltage. This is confirmed by the small C_1/C_0 requirements of our example. From (9) and (10), a peak-to-peak pump voltage of only 16 mV is needed to sufficiently perturb the varactor so that a 10 MHz bandwidth is established. This must be tempered with the fact that in this case the pump needs to operate at 60 GHz which is not out of the question for production level technologies (albeit a significant stretch for CMOS) exploiting distributed operation [13], frequency doubling [14], or second-harmonic generation [15]. Further, it is possible to redesign the pumping scheme of the parametric converter to continue meeting the Manley-Rowe predictions while operating with a pump at lower frequencies. This is discussed in Section 3.3.

The benefits available to the USBUC become serious impairments when considering this topology for a receiver's downconversion block. The substantial gain available to the upconverter (7) becomes a tremendous loss as, naturally, $f_u \ll f_s$ for downconverters. Fortunately, a large variety in parametric conversion topologies exists, some of which do allow for gain in the downconversion arrangement. One such topology is discussed presently.

3.2. Lower-sideband downconverter

The lower-sideband downconverter (LSBDC) is one parametric topology capable of amplifying a signal mixed down to the intermediate frequency (IF) or baseband (BB). In this

case, the converter's cavity is aligned such that power only at f_s (the RF signal), f_p, and $f_d = f_p - f_s$ (the downconverter signal) can flow through the circuit. To obtain a low-frequency output, the constraints $f_p > f_s$ (otherwise an upper-sideband downconverter is realized) and $f_p < 2f_s$ (otherwise a lower-sideband upconverter (LSBUC) is realized) must hold. Returning to the Manley-Rowe relations we get

$$\frac{P_{1,0}}{f_s} + \frac{P_{1,-1}}{f_s - f_p} = \frac{P_s}{f_s} - \frac{P_d}{f_d} = 0, \tag{11}$$

$$\frac{P_{0,1}}{f_p} + \frac{P_{-1,1}}{-f_s + f_p} = \frac{P_p}{f_p} + \frac{P_d}{f_d} = 0. \tag{12}$$

Adding (11) and (12) results in

$$\frac{P_p}{f_p} + \frac{P_s}{f_s} = 0 \tag{13}$$

which, given that the pump power flows into the circuit, implies that power emerges from the converter's input (signal) port despite an input signal being fed into the receiver (e.g., from an antenna). Hence, the impedance of the LSBDC's signal port is negative. Similarly, (12) states that the pump energy causes power to emerge from the downconversion port as well. Being related to the power emerging from the signal port (see (11)) this implies that the downconversion port impedance is also negative. The LSBDC doubles as a reflection amplifier.

The operation of this circuit can be summarized as follows. The pump generates the highest frequency "signal" in the circuit. Thus, unlike the USBUC, on average it can couple power from the signal port (RF) to the downconversion port (IF) and vice versa. As with the USBUC, the power coupling and amplification is mitigated by work done by the pump in changing the varactor capacitance. Since the pump switches only slightly faster than the signal, it transfers a relatively small amount of the input power into the downconversion port's IF frequency. However, being much higher than IF, the pump taps, amplifies, and converts a great deal of the IF back to RF (as predicted by (11)). Part of the larger input signal is then tapped once again by the pump and fed into the downconversion port. A positive feedback is established and the circuit functions as a regenerative amplifier. Thus the pump power emerges as RF and IF frequencies from the respective ports which now have a negative input resistance. The more power that is pumped into the circuit is, the higher the quality factor, Q, of the RF and IF modes is. Thinking of the input as a forcing signal on these modes we can automatically see that the higher the Q, the higher the signal gain, but the lower the bandwidth. Nonetheless, for signals centered around millimeterwave carriers, the LSBDC topology has a lot of relative bandwidth performance to sacrifice. What is a drawback to this circuit, however, is that an excess of pump power leads to instabilities (overcompensation of loss) and, simultaneously, a greater sensitivity to component variations (thus increasing the likelihood of instability). However, the advantage remains the potentially low-noise behavior about which the Manley-Rowe relations say nothing. We return to this in Section 5.

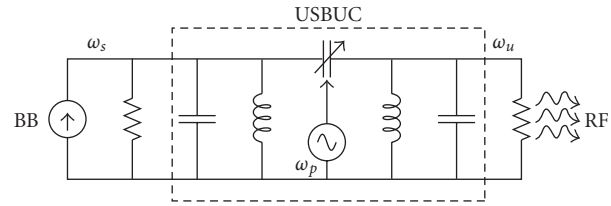


Figure 2: A simple transmit chain employing the USBUC.

3.3. Parametric transmit and receive chains

How can parametric converters be assembled into the transceiver chain? Since they combine oscillator, mixer, and amplifier functions under essentially one circuit, they hold the potential to form the basis for a diverse set of radio systems.

Perhaps the most straightforward application is the use of an USBUC as a low-voltage upconverter of BB or IF signals to millimeter RF. For minimal complexity and power consumption, the design in Figure 2 can be used. This diagram suggests interfacing the USBUC directly to the antenna which, if the antenna is sufficiently narrowband, can serve as the upper-sideband bandpass filter. Employing a standard two-terminal varactor structure in this topology will impose extra gain limiting—significant upconverted signal amplitudes can induce lower-sideband signals to flow (i.e., $\omega_p - \omega_s$) thus returning power back to the input source. A simple alternative is to use the USBUC as an upconverting mixer and preamplifier and leave the final millimeter wave amplification to a dedicated high-frequency (and high-cost) power amplifier. Alternatively, a double-balanced varactor structure (as described in Section 4.3 in the context of VCO frequency control) can be used in an attempt to desensitize the varactor capacitance to variations in the upconverted signal frequency.

Another transmitter topology shown in Figure 3 incorporates a degenerate local oscillator (LO) in a heterodyne USBUC architecture. In this case, the gain of the USBUC is distributed over several stages. The benefit of such a partition is reaped by the pump which can potentially be generated in a staged fashion as well. In Figure 3 the staged pump is built out of degenerate parametric converters. In degenerate converters, the signal (i.e., the LO) acts simultaneously as the input and the pump. A self-mixing occurs which naturally results in a signal at twice the input frequency. As shown, two such stages attached back-to-back can produce a signal at four times the driving pump frequency (with the need of a high power output at ω_p) and be combined with a multistage USBUC to gradually upconvert a signal from ω_s to $7\omega_p + \omega_s$.

Since parametric circuits couple power from low to high frequencies, the receiver's downconversion function obviously poses a problem. As already described, the LSBDC gets around this by employing positive feedback which can give substantial gain at the expense of sensitivity. A possible receiver topology employing a LSBDC is shown in Figure 4. Since the circuit functions as a reflection amplifier for both RF and IF frequencies, a circulator is included to prevent

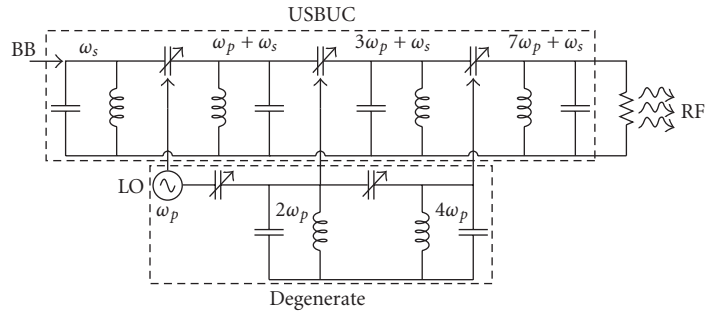


Figure 3: Multistage USBUC transmitter with degenerate pump.

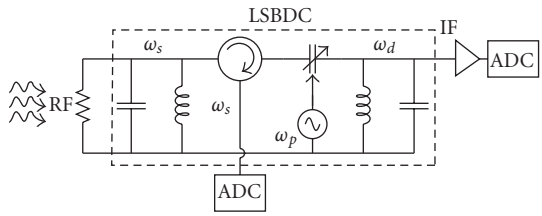


Figure 4: Receive chain using a LSBDC as a mixer and amplifier.

re-radiation and help maintain stability. A number of options are available even within the basic LSBDC receiver. Most simply it can be treated as a low-noise amplifier (LNA) and the amplified RF signal tapped out of the circulator to the remainder of the radio. In this case we benefit simply from the large gain and low-noise performance of the parametric converter. Any standard downconversion architecture or subsampling techniques can be employed afterwards. Compared to integrated transistor LNAs operating in the microwave region this benefit is marginal at best. However, at millimeter wave frequencies the improvements for amplification, noise, and power consumption become marked (at least compared to production-level CMOS technology). Using the downconversion port is another possibility, in this case taking advantage of the LSBDC's conversion properties alongside its low-noise performance. The difficulty in this case is gain, as the downconversion gain is increased, the regenerative design becomes difficult to stabilize under practical conditions.

An obvious issue with parametric converters is the high pump frequency needed to transfer power. As a result, a number of high-frequency pump generation and conversion techniques have already been mentioned. Another approach is to reconfigure the varactor structure for subharmonic pumping. Subharmonic pumping refers to an arrangement in which a certain pumping frequency transfers energy at the same rate as would a higher pumping frequency.

The subharmonic pumping suggestion does not pose an immediate violation of the Manley-Rowe relations. Rather, one means of its realization is to simply utilize one of the higher pumped capacitance harmonics [16]. Herein, the more abrupt MOS CV characteristics (compared to the junction varactor) can be of substantial benefit. For example, imagine a varactor pumped such that part of its Fourier series expansion from (8) is

$$C_A(t) = \cdots + C_{-2}e^{-j2\omega_p t} + C_{-1}e^{-j\omega_p t} + C_0 + C_1 e^{j\omega_p t} + C_2 e^{j2\omega_p t} + \cdots . \tag{14}$$

Another varactor, C_B, pumped 180° out of phase relative to C_A can be described with

$$C_B(t) = \cdots + C_{-2}e^{-j2(\omega_p t+\pi)} + C_{-1}e^{-j(\omega_p t+\pi)} + C_0 + C_1 e^{j(\omega_p t+\pi)} + C_2 e^{j2(\omega_p t+\pi)} + \cdots . \tag{15}$$

Combining C_A and C_B,

$$C_A(t) + C_B(t) = \cdots + C_{-2}e^{-j2\omega_p t} + 2C_0 + C_2 e^{j2\omega_p t} + \cdots , \tag{16}$$

leads to a net capacitance variation occurring at twice the actual pump rate. The schematic of a differentially driven subharmonic scheme based on this approach is shown in Figure 5. For subharmonic pumping to actually work here the varactors, C_A and C_B, must both have the same terminal (either gate or source) connected to the circuit proper. Aside from exciting the second harmonic, the differential pumping scheme allows the circuit to operate without a dedicated pump filter despite the use of two-terminal varactors. Alternatively, if the orientation of one varactor is flipped (i.e., terminal connections reversed or a complementary structure used) the subharmonic pumping effect is removed. The benefit of this connection, however, is the isolation of any pump frequencies from the signal and output ports allowing the filtering at these terminals to be significantly relaxed.

A more extreme attempt at subharmonic pumping employing a four-phase excitation scheme is sketched in Figure 6. In this case a ring oscillator (an injection locked oscillator can be used for better purity) generates differential in-phase and quadrature signals. Altogether four pump signals offset by 90° are available. Each pumping signal is sent to a separate varactor with CV characteristics identical to the other three. Given sufficiently nonlinear (i.e., abrupt) CV characteristics

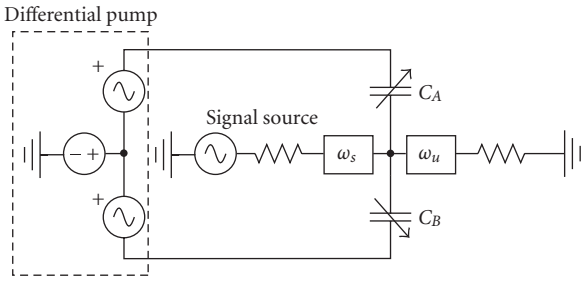


Figure 5: A differential subharmonic pumping scheme.

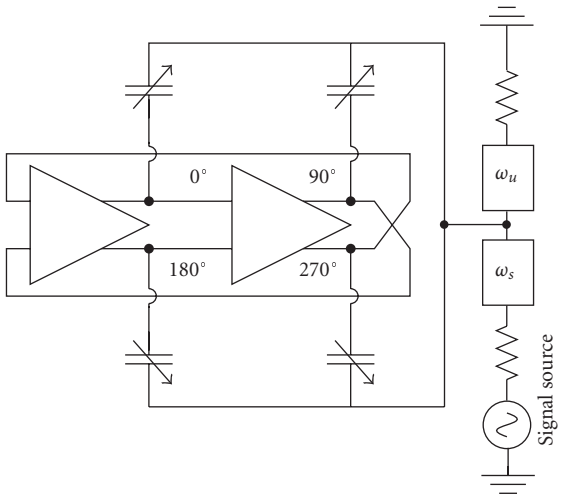


Figure 6: A possible four-phase subharmonic pumping scheme.

the net capacitance seen between the signal (ω_s) and upconversion (ω_u) terminals of the varactor will vary at four times the injected pumping frequency. Of course, at this harmonic, a large degradation in capacitance can be expected compromising the benefit of low pumping frequencies.

4. VARACTOR STRUCTURES

Since the late 1950's the junction diode has served as the de facto standard for all electronic parametric amplifiers. However, in parametric structures, and for oscillator frequency control, the junction diode is generally inferior to MOS varactor structures. Since the most vigorous research on electronic parametric circuits predates the rise of MOS technology, they have only sporadically been considered in the context of modern electronic technologies (and their applications); [9] is a rare example. In this section we look closer at the key varactor characteristics and design options for RF frequency control and parametric conversion.

4.1. Elastance model

An important advance in customized MOS varactor technology for RF applications was taken when CMOS processes

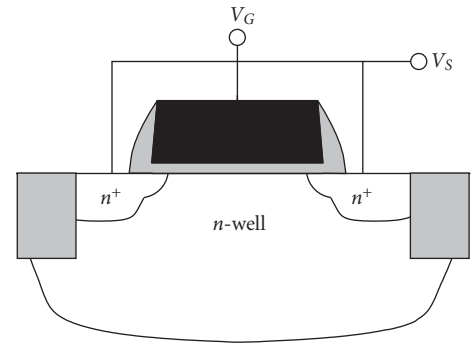


Figure 7: A sketch of an n-type (referring to the body doping) accumulation-mode varactor's cross-section.

began to accommodate the accumulation-mode varactor [17, 18] (Figure 7). This simplified the device bias scheme as compared to the more common inversion-mode varactor and simultaneously lowered its resistive losses and parasitic contributions. As a frequency tuning element the advantages of the accumulation-mode varactor compared to the junction diode were clear, a large $C_{\max}/C_{\min}$ ratio, an abrupt capacitive transition implying only the need for low tuning voltages, an isolated bias scheme, and acceptable Q. Optimization of these characteristics for LC-VCOs are straightforward: one must increase the $C_{\max}/C_{\min}$, and reduce resistive losses. For parametric circuits a more detailed assessment is necessary.

First, unlike Manley-Rowe, a more accurate analysis of parametric circuit behavior must account for losses in the varactor. To this end a rough but physically realistic pumped varactor model employs a nonlinear capacitance in series with a resistance, R_s. As emphasized by Penfield and Rafuse [19] this varactor model sidesteps the difficulties and inaccuracies that emerge when a parallel RC equivalent is used or when the series resistance is incorporated into source and load impedances. The terminal characteristics of this physically motivated model are best described with the relation

$$v(t) = \int S(t)i(t)\mathrm{d}t + R_s(t)i(t). \tag{17}$$

This equation directly catalogues the influence of the pump voltage on the varactor as a whole. However, it contains a relatively obscure varactor measure, the incremental elastance, $S(t)$.[1] A rough approximation of a MOS varactor elastance per unit area is given by

$$S(V_{GS}) = \frac{Q_{sd}(V_{GS})}{e\epsilon_s N_d} + \frac{1}{C_{ox}}, \tag{18}$$

where C_{ox} is the oxide capacitance, e is the electronic charge, ϵ_s is the permittivity of the semiconductor, N_d is the donor

[1] For the remainder of the paper we refer to $S(t)$ as simply the elastance, with the incremental properties of this value remaining implicit. As with the capacitance of nonlinear devices, practical measurement techniques allow the extraction of only incremental properties.

doping in the semiconductor (a uniformly doped n-type accumulation-mode varactor is assumed), and Q_{sd} is the depletion charge in the semiconductor body. The depletion charge itself is modeled semi-empirically with

$$Q_{sd} = \frac{e\epsilon_s}{C_{ox}N_d}\left(\sqrt{1+\frac{4V_{\mathrm{MOS}}}{\gamma^2}}-1\right), \tag{19}$$

where γ is the device body factor and

$$V_{\mathrm{MOS}} = \frac{1}{2}\left[\sqrt{(V_{GS}-V_{FB})^2+\delta}-(V_{GS}-V_{FB})\right]. \tag{20}$$

The above follows a modeling technique reported in [20] and, as in that work, incorporates a small smoothing factor, δ. This correction is used since the transition from full accumulation to flat-band is not rigorously accounted for here. With such factors present it is best to consider this model as a rough design guide. A detailed account of the varactor device physics in compact model form is described in [21] for example. The value of the simple model described here lies in its direct exposure of the relations between performance and device characteristics. Section 4.2 discusses this, along with device losses, in detail.

A comparison of this approximation to the normalized CV and SV characteristics extracted from a full charge-based analysis [22] as well as a simple tanh curve fit is presented in Figure 8. As shown, the tanh curve, a popular approach in empirical compact CV models, underestimates the elastance in depletion. We return to this point in Section 4.2.

4.2. Figures of merit

The elastance characteristics must be considered along with device losses in estimating the impact of integrated MOS technology on parametric performance. Penfiled and Rafuse [19] highlighted two figures of merit, the *cutoff frequency*

$$f_c = \frac{S_{\max}-S_{\min}}{2\pi R_s} \tag{21}$$

and the *modulation ratio*

$$m_n = \frac{|S_n|}{S_{\max}-S_{\min}}. \tag{22}$$

The cutoff frequency, which we can express in more familiar varactor measures as

$$f_c = \frac{C_{\max}-C_{\min}}{2\pi R_s C_{\max}C_{\min}}, \tag{23}$$

reflects only the influence that device properties bear on the circuit. Ideally, f_c marks the maximum frequency at which it is worth pumping the capacitor. Conversely, the modulation ratio encompasses several contributions. The numerator, $|S_n|$, indicates the size of the elastance harmonic at the pumping frequency $n\cdot f_p$. That is, assuming small-signal conditions, we can treat the elastance as a linear time-varying component controlled by the pump

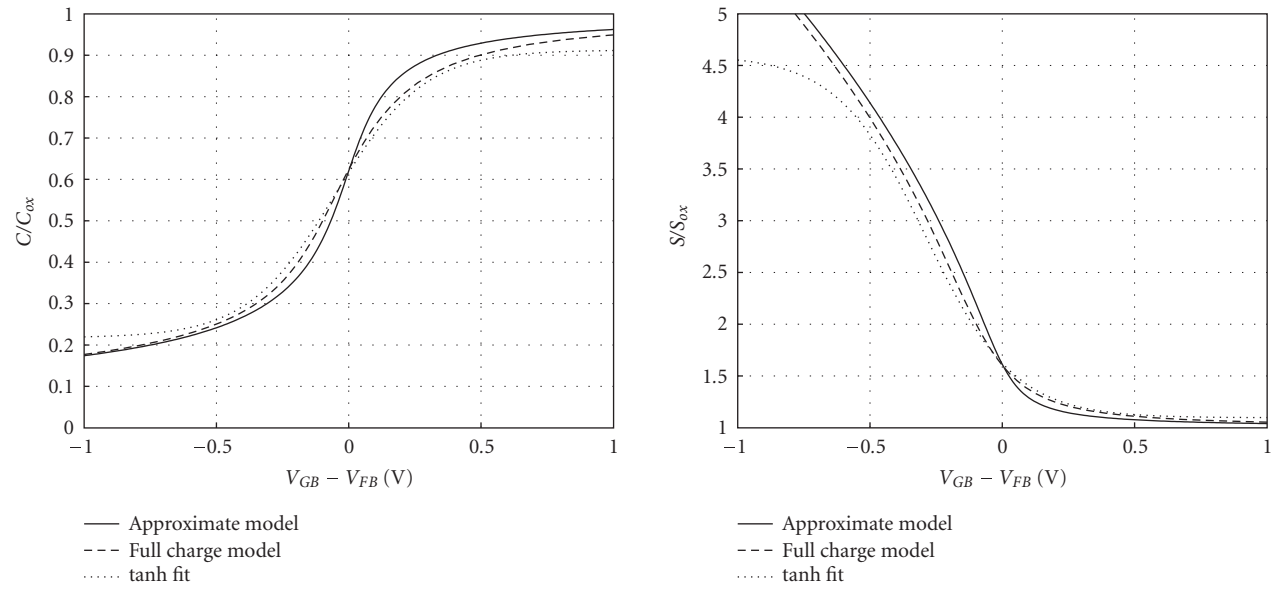
$$S(t) = \sum_{n=-\infty}^{\infty} S_n e^{j2\pi n f_p t}. \tag{24}$$

This is the elastance analog to (8). The elastance harmonics are influenced by three things: the bias of the pumping signal, the amplitude of the pumping signal, and the steepness of the varactor's elastance characteristics. The steeper the SV curve is, the more efficient the pump is in relaying its energy to the varactor. As shown in (18) and (19) a large impact on the abruptness of the elastance characteristic can be made by reducing the channel doping. This necessarily increases the series losses, but at a rate proportional to N_d, while the SV slope increases with N_d^2. Similarly, we can see from (19) that a decrease in the gate capacitance per unit area, C_{ox}, also contributes to an improvement in the SV slope. This also comes with the benefit of allowing larger pumping signals to be applied across the gate oxide.

These relationships run in a direction counter to the changes employed in scaling MOS devices. Nonetheless the variety present in most modern MOS technologies presents some room for optimization. For instance, many CMOS processes offer devices of various oxide thickness and channel doping. A plot of the SV characteristics extracted from S-parameter measurements on accumulation-mode devices in a 0.13 μm-CMOS technology with varying channel doping and oxide thickness is shown in Figure 9. In this case only devices with a marginal difference in oxide thickness were examined. As expected, a lower channel doping results in a steeper SV characteristic. The measured 4-to-1 ratio between $S_{\max}$ and $S_{\min}$ is about 2.5 times greater than that available from a junction diode. The two channel doping levels (nominal and high) are obtained by employing threshold adjust implants intended for the variety of NMOS and PMOS devices offered in the technology. Unfortunately, a fourth experiment employing one of the available counterdoping implants and intended to have the lowest channel doping was not correctly processed at the foundry. This, correctly combined with the thick-oxide option available in most CMOS technologies, constitutes the most direct approach to device customization for parametric circuit applications.

Of note in the measurement results is the manner in which the elastance characteristic saturates in the depletion region. This is a characteristic encompassed by the tanh fit example included in Figure 8 but not the basic model of (18). The disparity between the predicted and measured elastance characteristics at large depletion bias can be traced to the fact that the varactor measurements were done with a small-signal, high-frequency (5 GHz) perturbation atop a slowly stepped bias—a common high-frequency CV extraction technique [23]. Such a set-up allows minority charge to respond to the bias settings thus preventing the onset of deep depletion as naturally included by the basic model. However, in parametric circuit applications we can expect a large-signal, high-frequency pump voltage to continuously excite the MOS varactor. Thus, the equilibrium bias conditions present during measurement hardly apply for pumped varactors. This supports the elastance predictions of the basic varactor model, but a convincing answer requires an analysis beyond the scope of this paper.

As highlighted by the merit relations, SV performance alone is not a sufficient device selection criterion. Careful



(a) Capacitance-voltage characteristics

(b) Elastance-voltage characteristics

Figure 8: Comparing the rough semi-empirical model to a complete charge-based description and a tanh fit.

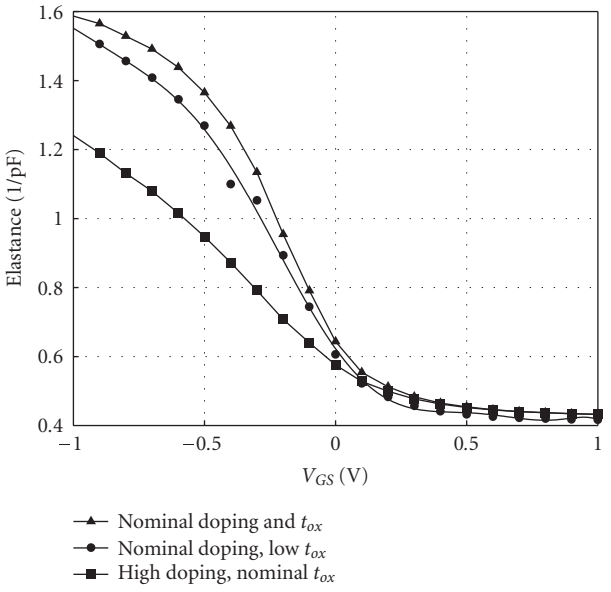


Figure 9: Elastance measurements for accumulation-mode varactors with varying degrees of channel doping in a 0.13 μm-CMOS technology.

consideration must be given to the reduction of series losses as attested by (23). For designers, with little control over the varactor's physical characteristics, layout becomes paramount here. Without considering special layout techniques (such as differential excitation [24]), four controls are available: gate length (L_g), gate width (W_g), finger number (N_f), and number of stripes/segments (N_s). These combine to give an active varactor area of $L_g \cdot W_g \cdot N_f \cdot N_s$. To clarify, a varactor consists of N_s stripes in parallel, each containing N_f fingers, in turn, each finger has dimensions W_g and L_g. We must consider what arrangement of these terms maximizes f_c. This requires finding the right balance between layout influence on series resistance and capacitance properties.

The series resistance can be divided into two main contributors, one is a constant value and is associated with the silicided poly gate, contacts, and via resistance on the terminals. The other contributor is associated with the channel material and is bias, doping, and frequency dependent.

For the accumulation-mode varactor with one finger, its series RC components can be modeled as in Figure 10, where R_{cg} and R_{csd} are the contact and via resistances on the poly gate and n^+ diffusion pickups (source/drain), respectively, and R_g is the gate polysilicon resistance. Underneath the gate, the channel resistance is denoted by R_{ch}, while R_w is the resistance of the n^+ diffusion bulk pickups and the well. C_{var} is the equivalent series capacitance of each finger. The model of the varactor with multiple fingers is shown in Figure 11, where R_{sfg} and R_{sfsd} are the series resistance between two fingers.

For the gate resistance, if the gate poly of each finger is joined from both sides of source/drain, the equivalent poly resistance of one finger is

$$R_g = \frac{1}{12} \cdot \frac{W_g}{L_g} \cdot R_{g-\text{sh}}, \tag{25}$$

where $R_{g-\text{sh}}$ is the gate's sheet resistance. On the other hand, for the channel and well resistance we have

$$R_{\text{ch}}, R_w \propto \frac{L_g}{W_g} \cdot R_{\text{ch},w-\text{sh}}. \tag{26}$$

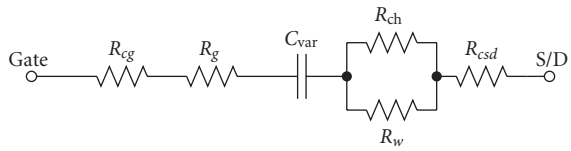


Figure 10: Model of a single-finger varactor.

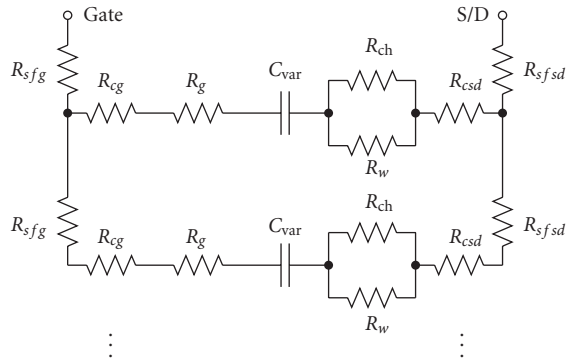


Figure 11: Model of a parallel multiple-finger varactor.

Being lower doped and unsilicided, the sheet resistance of the well and bulk, $R_{ch,w-sh}$, is greater than that of the polysilicon. This suggests that one would use the minimum channel length to reduce the body contribution to the series resistance. However, due to their inverse dependence on finger dimensions some tradeoff between the influence of (25) and (26) on the series resistance is present. This tradeoff affects the setting for W_g and L_g, but it is not the only consideration.

As shown in (23) we want to maximize C_{max}, minimize C_{min}, and minimize R_s. Somewhat arbitrarily choosing a minimum practical value of $C_{min} = 100$ fF (in anticipation of parasitic effects and process variations) we are left to consider how L_g, W_g, N_f, and N_s influence the remaining two characteristics, obviously this complicates selection based purely on an R_g-R_{ch} tradeoff. For instance, minimizing $L_g \cdot W_g$ maximizes the $N_f \cdot N_s$ product and therefore reduces R_s, but at the cost of increasing the relative parasitic capacitance contribution and hence a reduction in $C_{max} - C_{min}$.

Another important consideration is the contact and interconnect resistance introduced between fingers (R_{sfg} and R_{sfsd} in Figure 11) and stripes. This is often ignored when assessing device resistance, but can certainly be influential. With R_{sfg} and R_{sfsd} the equivalent resistance will not be reduced simply as a function of $1/N_f$. As N_f is increased the series resistance will eventually saturate due to the contributions of the interfinger connections, R_{sfg} and R_{sfsd}.

Getting a sense of how the characteristics L_g, W_g, N_f, and N_s influence f_c is greatly aided by the availability of verilogA based compact models such as the one described in [21]. Since these models account for both physical and layout characteristics a broad comparison between designs can be made. Employing empirically based compact models the f_c for a variety of accumulation-mode n-type varactors (excited in a single-ended manner) is shown in Tables 1–3. The total active area ($L_g \cdot W_g \cdot N_f \cdot N_s = 43.2\,\mu m^2$) is the only value that all designs have in common. It is chosen such that C_{min} remains above 100 fF over the relevant region of operation (V_{GS} ranges from -1 V to 1 V). Table 1 summarizes the results for varactors consisting of minimum unit area (i.e., $W_g \cdot L_g$) elements, Table 2 shows the results for devices composed of twice the minimum unit area, and Table 3 summarizes the characteristics of varactors composed of four times minimum unit area elements. Note that all R_s have been calculated for 5 GHz excitations. A layout dependent self-resonance frequency could not be extracted as the model did not account for inductive parasitics although it should be noted that self-resonant frequencies do not necessarily pose a problem for parametric circuits. The self-resonant frequency can be exploited as one of the modes of interest in the parametric circuit.

The f_c values shown are certainly optimistic as the compact models do not account for the effects that would limit device performance at such frequencies, nevertheless they are useful as a relative measure of the best device type. Judging by the f_c results, it is best to use an intermediate unit area that ably juggles two conflicting characteristics: parasitic capacitance and series resistance. For a given total area, as the unit

Table 1: Cutoff frequencies for varactor with $W_g = 1\,\mu$m, $L_g = 0.24\,\mu$m, and area = $43.2\,\mu m^2$.

N_f	N_s	C_{max}(fF)	C_{min}(fF)	$R_s(\Omega)$	f_c(GHz)
180	1	477.8	187.3	13.77	32.57
60	3	481.5	188.1	2.429	212.2
30	6	481.8	188.3	0.8025	641.5
15	12	482.3	188.7	0.508	1011
5	36	483.5	190	1.275	399

Table 2: Cutoff frequencies for varactor with $W_g = 1.41\,\mu$m, $L_g = 0.34\,\mu$m, and area = $43.2\,\mu m^2$.

N_f	N_s	C_{max}(fF)	C_{min}(fF)	$R_s(\Omega)$	f_c(GHz)
90	1	475.8	147.5	7.281	102.2
45	2	476.3	147.8	2.777	267.5
30	3	476.5	147.8	1.538	482.8
15	5	476.8	148.1	0.7094	1045
5	18	477.5	149	0.9085	808.9

Table 3: Cutoff frequencies for varactor with $W_g = 2\,\mu$m, $L_g = 0.48\,\mu$m, and area = $43.2\,\mu m^2$.

N_f	N_s	C_{max}(fF)	C_{min}(fF)	$R_s(\Omega)$	f_c(GHz)
45	1	475.8	147.5	4.359	222.8
5	9	476.3	122.1	0.9787	982.9
15	3	477.5	123.5	1.266	754.4

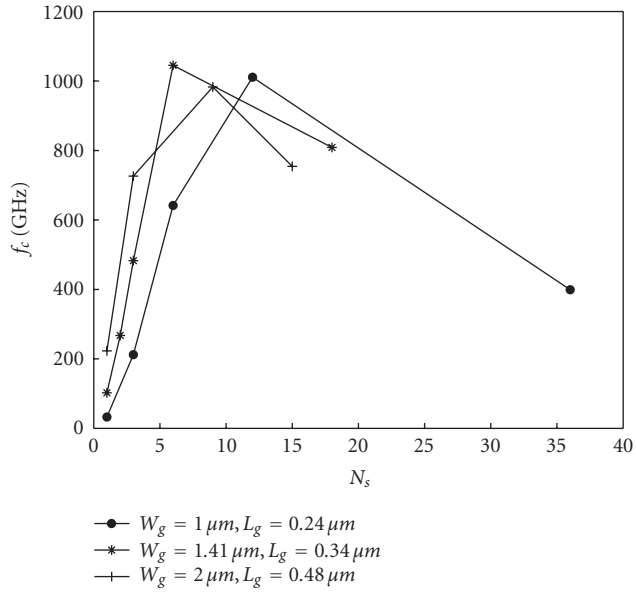


Figure 12: Plot of varactor cutoff frequencies versus number of stripes for a 43.2 μm^2 (total active area) varactor.

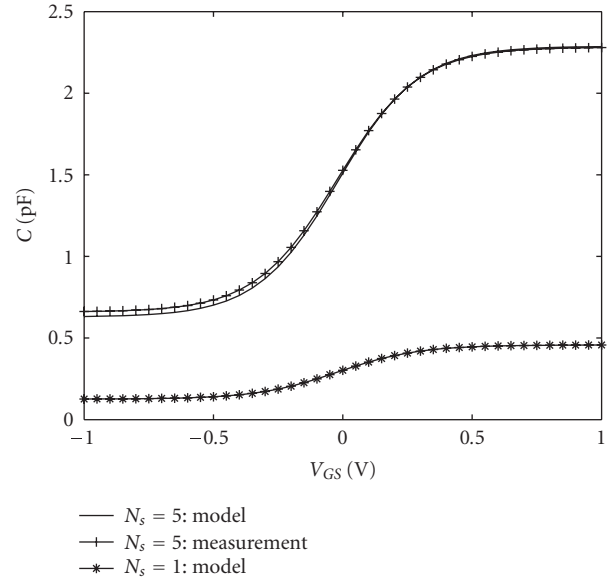


Figure 13: Comparison of measurement results to compact model predictions.

area shrinks, more devices in parallel imply a smaller total resistance. As can be seen in all cases, this is best achieved by keeping N_f and N_s on the same order. Unfortunately, the capacitance of small unit areas contains a higher relative proportion of parasitic capacitance. This lowers $C_{\max} - C_{\min}$ which ends up hurting the f_c. Attempts to get around this by increasing the unit area will be frustrated by an increase in series resistance simply due to a decrease in the parallel connection count. The simulated cutoff frequencies associated with these varactors are plotted in Figure 12 as a function of stripe count. As can be seen, f_c is relatively forgiving of unit size, but quite sensitive to N_f and N_s distributions.

Measured results are available to double-check the CV characteristics of the scalable varactor model. The experimental varactor design has unit widths and lengths of 5 μm and 0.42 μm, respectively, which are arranged into $N_s = 5$ parallel stripes of $N_f = 20$ gate fingers each. In Figure 13, the CV curve obtained from the model is plotted alongside the CV data obtained from a high-frequency (5 GHz) S-parameter characterization of the varactor. It is observed that the CV characteristic of the fabricated device matches very closely with the scalable model (at the frequency of extraction).

We will attempt to tailor this varactor design for parametric circuits by changing the number of stripes from 5 to 1. The implications of this change on the device characteristics and USBUC and LSBDC are explored in detail in Section 5. Even though reducing N_s will shift the CV curve down and decrease the $C_{\max} - C_{\min}$ (as shown in Figure 13), $C_{\min}$ has also been reduced thus increasing f_c. The large change in capacitance characteristics from $N_s = 5$ to $N_s = 1$ affects the performance quality of the parametric converter but not the substance of its operation, unlike, for example, that of a VCO, whose center frequency and tuning range would be severely impacted. The only requirement imposed in this work is that $C_{\min}$ exceed 100 fF, which has been satisfied.

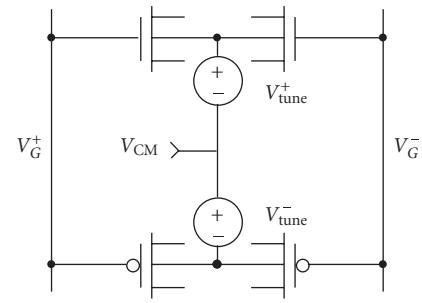


Figure 14: Schematic of common-mode cancellation varactor.

4.3. Composite structures

Besides refining layout, useful varactor customization can be achieved by connecting devices for optimal excitation. An example of this is the work reported in [24] where varactors subject to differential excitation (e.g., in a differential VCO) profit from a virtual ground connection which reduces the effective series losses. Another possibility is the common-mode rejection architecture [25]. In this case, varactors are arranged such that they respond symmetrically to differential excitations, but in an antisymmetrical manner to common-mode excitations thus damping the latter's influence. This can be useful for both parametric converters (allowing large signal operation) and VCOs (removal of supply disturbances). A discussion of the latter is given in Section 6.

A schematic of the proposed varactor circuit is shown in Figure 14. In effect, this arrangement resembles the basic

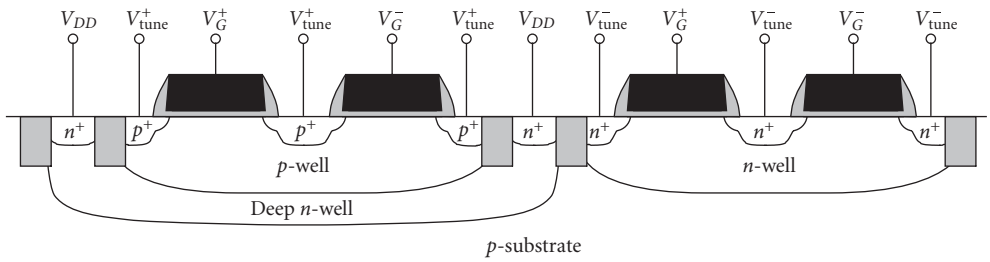


Figure 15: A sketch of the cross-section of a common-mode-cancellation accumulation mode varactor. Compare this to the schematic of this "device" rendered in Figure 14.

antiparallel connection (i.e., a pair of two-terminal asymmetrical devices connected in parallel, but with opposite terminal orientations) [26]; in practice, it isolates the differential V_G node from the substrate losses. Isolating sensitive nodes from the substrate is much less of a concern in the case of an SOI technology, but it is essential in a CMOS technology where such a load can severely degrade the tank Q in LC-VCOs. A common-mode rejection varactor (CMRV) circuit, consisting of n-type and p-type accumulation-mode varactors, can be realized in any CMOS technology with a deep n-well. The deep n-well doping is used to define an isolated p-well and hence the p-type accumulation mode varactor needed to complement the n-type varactor. Further, it is possible that such a device can be tightly integrated into one composite structure as illustrated in Figure 15. As sketched, the device also takes advantage of a differential excitation layout to help reduce series losses.

At present, CMOS processes commonly include n-type accumulation-mode devices, however it is uncommon to find the p-type corollary needed in the CMRV. To approximate the properties of such a pair, the 2D device simulator, MEDICI, is employed. The construction of the hypothetical p-type device is guided by the approximated doping levels of an n-type varactor available in a 0.13 μm-CMOS technology. The doping levels are simply mirrored.

The CV characteristics obtained for the n-type and p-type accumulation mode varactors using MEDICI are shown in Figure 16. Apparently, a relatively antisymmetric response is possible if matched doping levels are used in the two devices. Simulator mesh size limits required a separate analysis for each varactor flavour, nonetheless the results are expected to be indicative of the fully integrated device operation. The benefits that such a device brings to VCO phase noise behavior in the presence of extrinsic disturbances are discussed in Section 6.

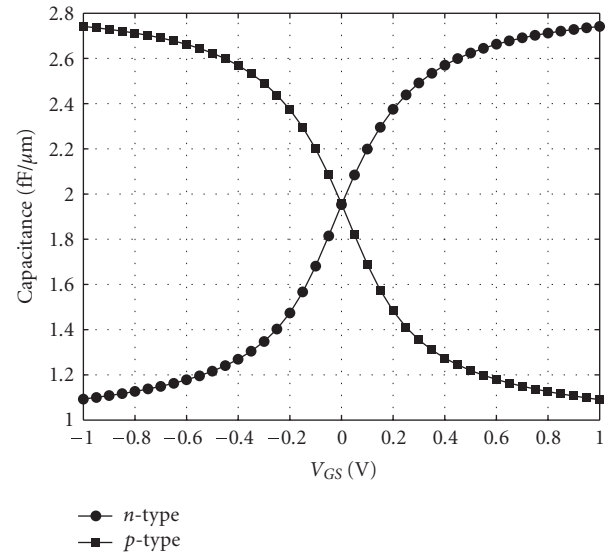


Figure 16: Comparison of MEDICI simulated CV characteristics of matched n-type and p-type varactors.

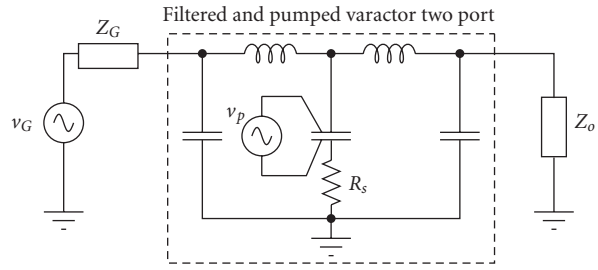


Figure 17: The upper-sideband upconverter represented as a two port with ideal filters and series loss, R_s only in the varactor.

5. PARAMETRIC CIRCUIT SIMULATIONS

5.1. USBUC

Although useful as a general guide, the predictions of the Manley-Rowe relations apply only to the case of a lossless reactance. Penfiled and Rafuse [19] emphasized the need to account for series varactor losses when evaluating parametric circuit performance. Following this work, the available gain of an USBUC treated as a two port (see Figure 17) is given by

$$\frac{1}{G_a} = \left(\frac{\omega_s}{m_1\omega_c}\right)^2 \frac{|Z_G + R_s - jS_0/\omega_s|^2}{R_s R_G} + \frac{\omega_s}{\omega_u}\frac{R_s + R_G}{R_G} \tag{27}$$

assuming that only (angular) frequencies ω_s, ω_p, and $\omega_u = \omega_s + \omega_p$ are allowed to exist in the cavity. The influence of

the cutoff frequency (in rad/s as ω_c) and the modulation index (m_1) is clearly seen here. Expecting the USBUC to be used in a millimeter wave communicator transmit chain, we are most interested in the conditions necessary for maximum gain. From (27) we find that maximum available gain is

$$G_{a,\max} = \left(\frac{m_1\omega_c}{\omega_s}\right)^2 \cdot \left(1 + \sqrt{\frac{(m_1\omega_c)^2}{\omega_s\omega_u} + 1}\right)^{-2} \tag{28}$$

when the jS_0/ω_s term is resonated out and the generator resistance is set to

$$R_G = R_s\sqrt{\frac{(m_1\omega_c)^2}{\omega_s\omega_u} + 1}. \tag{29}$$

The varactor structures described earlier (Figure 13) are now used to get a sense of the performance attainable by the USBUC. The simulated figures of merit for these devices are summarized in Table 4. A DC point (−200 mV) is chosen for the pump signal such that the device is biased evenly between $S_{\max}$ and $S_{\min}$. Also, the figures are extracted for a sinusoidal pump signal of 300 mV peak amplitude applied directly across the varactor (i.e., −6.5 dBm from a matched 50 Ω pumping source). This prevents the generation of higher-order harmonics which, under the circuit conditions considered here, do not contribute any useful power gain and may actually decrease it.

The simulation results for an USBUC that amplifies and converts a 1 GHz signal to a 60 GHz frequency are shown in Table 5. A number of conditions are examined and, for easy reference, compared to theoretical calculations of available gain. The results are determined for no input match ((27) with $Z_G = 50\,\Omega$), input conjugate match ($Z_G^* = R_s - jS_0/\omega_s$), and gain optimization "match" (28).

For the first two varactor simulations ($N_s = 5$ measured and modeled), we see that the gain is well below that predicted by the Manley-Rowe relations. We can attribute this to the fact that our upper-sideband frequency is greater than $0.427\,(m_1\omega_c)^2/\omega_s$ (a design variable for USBUCs, indicating the signal frequency at which the converter's available power gain begins to saturate [19]), in the case of the five-stripe varactor (i.e., measured and modeled). Therefore, this varactor is an unsuitable choice for the design we have presented, since we are pumping it at too high a frequency. The one-stripe varactor, with a composite merit figure ($m_1\omega_c$) more than twice as great does not exceed the above condition and comes within 15% of the Manley-Rowe prediction.

5.2. LSBDC

Once again, following [19], for the LSBDC, considering varactor losses, the exchangeable gain becomes

$$\frac{1}{G_a} = \left(\frac{\omega_s}{m_1\omega_c}\right)^2 \frac{\left|Z_G^* + R_s + jS_0/\omega_s\right|^2}{R_sR_G} - \frac{\omega_s}{\omega_d}\frac{R_s + R_G}{R_G}. \tag{30}$$

From this equation, we can see that it is possible for the available gain to be negative. However, for this to be possible, it is necessary that $\omega_s\omega_d < (m_1\omega_c)^2$. In general, as long as $\omega_s < m_1\omega_c$, we will have a negative gain.

Table 4: Relevant varactor measurements with $V_{dc} = -200$ mV and $V_p = 300$ mV (peak).

Design	S_0 ($\times 10^9/F$)	S_1 ($\times 10^9/F$)	R_s (Ω)	$m_1\omega_c$ ($\times 10^9$ rad/s)
$N_s = 5$, Measured	957.2	211.9	1.1	192.7
$N_s = 5$, Model	987.7	228.0	1.032	220.9
$N_s = 1$, Model	4938	1140	2.359	483.3

Table 5: Simulated USBUC power gain.

Design	Condition	$Z_G[\Omega]$	G_a (theory)	G_a (sim)
$N_s = 5$	No match	50	1.94	1.91
Measured	Conjugate	$50 + j152.3$	14.81	14.65
—	Gain opt.	$4.49 + j152.3$	36.93	36.26
$N_s = 5$	No match	50	2.25	2.21
Model	Conjugate	$50 + j157.2$	17.29	17.08
—	Gain opt.	$4.8 + j157.2$	38.75	38.61
$N_s = 1$	No match	50	1.1	1.09
Model	Conjugate	$50 + j785.9$	46.77	46.57
—	Gain opt.	$23.5 + j785.9$	49.07	48.94

Assuming that one LSBDC will do the job of an entire receiver front end (i.e., LNA, mixer, oscillator) its noise behavior becomes an important concern. The noise temperature of the LSBDC is given by

$$T = T_d\left[\frac{R_s}{R_G} + \left(\frac{\omega_s}{m_1\omega_c}\right)^2 \frac{\left|Z_G^* + R_s + jS_0/\omega_s\right|^2}{R_sR_G}\right], \tag{31}$$

where T_d is the varactor temperature. If we are planning on implementing this receiver system with an on-chip antenna, we can expect the antenna and the varactor to be roughly the same temperature. Thus the single-sideband noise factor will be

$$F - 1 = \left[\frac{R_s}{R_G} + \left(\frac{\omega_s}{m_1\omega_c}\right)^2 \frac{\left|Z_G^* + R_s + jS_0/\omega_s\right|^2}{R_sR_G}\right]. \tag{32}$$

As in the USBUC, the first step we can do to improve gain and noise performance is to perform a reactance match, which is done by letting $X_G = S_0/\omega_s$. As a result, the improved noise factor becomes

$$F - 1 = \left[\frac{R_s}{R_G} + \left(\frac{\omega_s}{m_1\omega_c}\right)^2 \frac{(R_G + R_s)^2}{R_sR_G}\right]. \tag{33}$$

Table 6: Simulated LSBDC performance.

Design	Condition	$Z_G(\Omega)$	Z_{out} (theory)	Z_{out} (sim)	NF (dB)
$N_s = 5$ Measured	No match	50	$0.73 - j152.4$	$0.73 - j144.4$	22.63
	Reactive match	$50 + j2.54$	$0.73 - j152.3$	$0.73 - j144.4$	22.62
	Noise opt.	$1.24 + j2.54$	$-7.02 - j152.3$	$-6.84 - j143.8$	12.37
$N_s = 5$ Model	No match	50	$0.603 - j157.2$	$0.609 - j148.3$	21.71
	Reactive match	$50 + j2.62$	$0.602 - j157.2$	$0.609 - j148.3$	21.70
	Noise opt.	$1.20 + j2.62$	$-8.82 - j157.2$	$-3.03 - j143.5$	11.33
$N_s = 1$ Model	No match	50	$-7.5 - j788.4$	$-7.3 - j737.5$	12.06
	Reactive match	$50 + j13.1$	$-8.1 - j785.9$	$-7.9 - j739.9$	11.82
	Noise opt.	$3.8 + j13.1$	$-86.22 - j785.9$	$-84.8 - j740$	6.23
$N_f = 15$ $N_s = 12$ Table 1	No match	50	$-2.41 - j582$	$-2.40 - j563$	10.6
	Reactive match 1	$25 + j9.7$	$-5.49 - j581$	$-5.45 - j563$	5.6
	Reactive match 2	$20 + j9.7$	$-6.95 - j581$	$-6.90 - j563$	4.3
	Reactive match 3	$15 + j9.7$	$-9.36 - j581$	$-9.29 - j563$	3.0
	Noise opt.	$1.7 + j9.7$	$-69.6 - j581$	$-68.3 - j563$	2.8

Furthermore, the source resistance can be tuned to improve the noise factor even more. Setting it to

$$R_G = R_s\sqrt{1+\left(\frac{m_1\omega_c}{\omega_s}\right)^2} \tag{34}$$

results in an excess noise factor of

$$F-1 = \frac{2\omega_s}{m_1\omega_c}\left[\frac{\omega_s}{m_1\omega_c}+\sqrt{1+\left(\frac{\omega_s}{m_1\omega_c}\right)^2}\right]. \tag{35}$$

As for the gain of the LSBDC, when the noise is optimized, the available gain is predicted to be

$$G_a = \sqrt{1+\left(\frac{m_1\omega_c}{\omega_s}\right)^2}\cdot\left[\frac{\omega_s}{m_1\omega_c}+\sqrt{1+\left(\frac{\omega_s}{m_1\omega_c}\right)^2}\right]^{-1} \cdot\left[\frac{\omega_s}{m_1\omega_c}+\sqrt{1+\left(\frac{\omega_s}{m_1\omega_c}\right)^2}-\frac{m_1\omega_c}{\omega_d}\right]^{-1}. \tag{36}$$

Thus, the available gain can still be negative under optimum noise matching conditions, implying that the LSBDC still has a negative equivalent output resistance and hence the ability to deliver power at the signal and downconversion ports. Note that in this case (optimum noise match), it is possible to increase the gain by changing the pumping frequency and hence ω_d; this option is somewhat limited when the LSBDC serves as a downconverter (as opposed to a straight LNA) since the IF frequency is not commonly a design variable on the circuit level.

As done for the USBUC, we examine the (noise) performance of the LSBDC with the same varactor structures and pumping conditions summarized in Table 4 as well as similar operating conditions (60 GHz input signal, 1 GHz downconverted signal). In Table 6, the theoretical and simulated output impedances along with the expected noise figure of each of the LSBDC circuits are given. Note that we present the output impedances as opposed to the available gain from the LSBDC. The reason for this is that the absolute value of gain can be smaller than one, yet gain will still be possible, depending on the load. Thus if we know the output impedance of the LSBDC, we can choose the loads appropriately to give the desired gain. Admittedly this is difficult to do in board-level designs, but certainly is not out of the question in high frequency integrated circuits where designers have much more control over the interface between circuits. In the case of the five stripe varactor (measured and modeled), when the source resistance is 50 Ω, the real part of the output impedance will actually be positive, and thus the LSBDC will operate with a power loss when using these varactors under the conditions in this analysis.

As shown in Table 6 the single strip device has a promising noise figure assuming that the source has been tuned for noise optimization. The optimum source noise resistance (3.8 Ω) is quite low for the particular version of the LSBDC studied here. Fortunately, the design is not impractically sensitive to source impedance variations. For example, a 600% increase in source resistance to 25 Ω results in a noise figure of 6.95 dB, a 0.72 dB increase. This compares favourably with the performance achieved using standard IC radio topologies. For instance, one report [27] describes a 60 GHz transceiver implemented in a 200 GHz f_T 0.12 μm SiGe technology with a measured 11 mW LNA noise figure of 4.5 dB and a 147 mW mixer (driven by a 30 mW VCO) with a noise figure of 14.8 dB. Importantly, it must be emphasized that the simulated parametric behavior reported here is managed with a simple circuit consisting, aside from an oscillator, entirely of passives. Further, the parametric converter is not heavily reliant on the quality of its IC technology, for instance, the noise performance estimated in Table 6 is built around a CMOS varactor with $L_u = 0.42\,\mu$m. Granted, this

analysis considers only the varactor's noise contribution, but it should be noted that the device under question is inferior to a number of other available device designs cataloged in Tables 1 to 3. Optimizing around one of the better varactors listed (specifically, the minimum unit area varactor with $N_f = 15$ and $N_s = 12$ in Table 1) predicts very encouraging results for the operational circumstances under consideration. An optimum noise figure of 2.8 dB is predicted under an optimum R_G of 1.7 Ω. This value increases to 3, 4.3, and 5.6 dB at more reasonable source resistances of 15, 20, and 25 Ω, respectively.

6. FREQUENCY CONTROL

A schematic of a simple cross-coupled CMOS LC-VCO structure is shown in Figure 18. The circuit incorporates the common-mode rejection varactor (CMRV) introduced in Section 4.3. Only one switching core is used to overcome tank losses, a PMOS cross-coupled pair. This allows the circuit to operate with low voltage supply headroom. Also, buried channel PMOS devices are employed for their lower flicker noise contribution.

In this case, the purpose of the CMRV is to maintain the large tuning range inherent to MOS varactors while simultaneously desensitizing the VCO to common-mode fluctuations induced by the supply noise. The CMRV allows a differential signal (e.g., $V^+_{\text{tune}} - V^-_{\text{tune}}$) to simultaneously excite the n- and p-type varactors into their depletion or accumulation regimes. Meanwhile, a common-mode excitation (e.g., V_{CM}) drives the two devices into opposite regimes of operation, thus blunting the overall response of the CMRV to that signal.

A substantial source of common-mode noise in modern mixed-signal environments is the rail noise at V_{DD} and V_{SS}. The PMOS current mirror ($M_3 - M_4$) helps block out V_{DD}-noise. However, ordinarily, the phase noise performance of this topology would be severely compromised by variations on V_{SS}. That is, any noise occurring on V_{SS} can be expected to lead to a large increase in the VCO phase noise. A comparison of this increase between a 5 GHz LC-VCO employing an n-type varactor and an identical VCO employing a CMRV over a tuning voltage spanning −1V to 1V is shown in Figure 19. Specifically, the change in spot phase noise at 1 MHz removed from the center frequency is compared using the SpectreRF simulator. In both cases (i.e., normal and CMRV tuned VCO) uniform low-frequency noise (0 to 20 MHz) is placed on V_{DD} and V_{SS} and sized such that the common-mode noise density (in V^2/Hz) induced by each noisy rail at a tank node is 70 dB greater than intrinsic VCO noise effect at that node. High-frequency extrinsic noise is less of a concern in this case as it can be more effectively suppressed by on-chip shunt capacitors.

For V_{SS} noise (solid line in Figure 19) the CMRV offers a substantial improvement. At best, the 1 MHz spot phase noise is more than 50 dB less sensitive to V_{SS} fluctuations on the CMRV tuned VCO. This occurs when the varactor is tuned within the CV transition region between accumulation and depletion regimes. Expectedly, as V_{tune} is changed

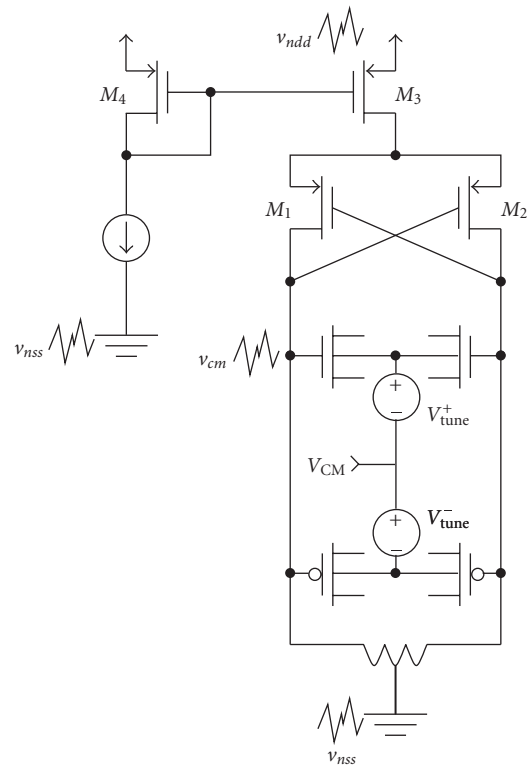


Figure 18: A simple CMOS LC-VCO with common-mode cancellation varactor.

and the CMRV biased in one of its saturated domains the common-mode cancellation effect is diminished. For V_{DD} fluctuations (dashed line in Figure 19) the CMRV offers little benefit in this topology. In this case, any noise that enters the common-source terminal of the cross-coupled PMOS pair through M_3 is converted to a differential form. As already stated, the CMRV does not filter out such excitations.

7. DISCUSSION

Customized varactor structures can help standard CMOS technology continue to meet more demanding RFIC challenges. In this paper we discussed the role that these devices can play in assisting millimeter wave signalling and frequency control in a mixed-signal environment. The former is addressed by suggesting the use of MOS varactors in parametric conversion circuits. This circuit approach is always an option when operational frequencies beyond the reach of transistor technology are the goal. The MOS varactor assists the efficacy of this technique with its rich nonlinearity (compared to the junction varactor), broad capacitive range, complementary structure (i.e., n-type and p-type varactor modes), three-terminal operation (not discussed in this paper), and unintrusive biasing.

Perhaps the most nagging issues with parametric circuits are their need for high pumping frequencies and copious filtering. A number of proposals were made in this work regarding these, from high-frequency reference generation, to subharmonic pumping, to differential excitation. These

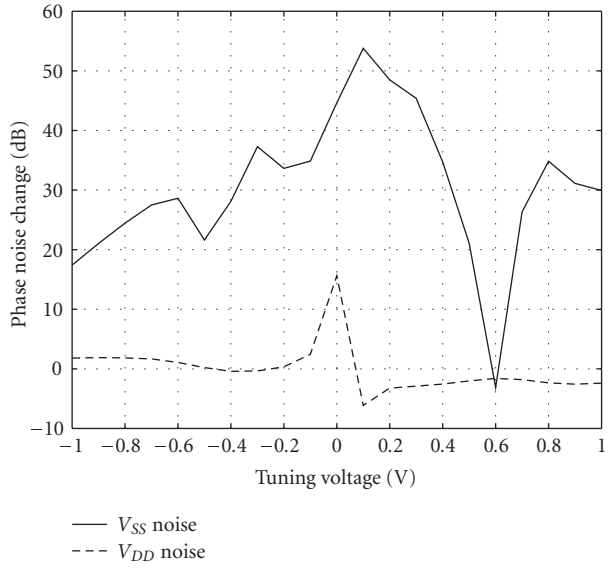


Figure 19: Simulated change in phase noise for single-ended and common-mode reject varactor structure.

approaches are aided by IC implementations (better matching) and the custom device structures (complementary varactors) which can be fabricated with only a layout rearrangement (i.e., without specific need for thermal budget or doping adjustments during processing). Suggestions were also made for customization of physical MOS varactor characteristics to better suit parametric needs. Given the availability of thick oxide analog devices in mixed-signal CMOS technologies and the presence of multiple threshold implants even this adjustment can be implemented without significant process demands.

Attention was also brought to several issues involving accumulation-mode varactors in parametric converters. The importance of elastance-based design was mentioned (e.g., this influences the optimum pump biasing) and a simple elastance model discussed. An outstanding point is the impact of nonequilibrium, deep-depletion effects. RF MOS characterization typically does not elicit this behavior, however it is expected to play a role in parametric circuit performance. An investigation into optimum device layout based on compact models highlighted the need to balance finger and stripe count of the varactor. Ignored were the possible influences of capacitive well parasitics on the frequency response of parametric ICs.

The effect of a complementary LC-VCO tuning scheme was also studied in simulation. A significant improvement in the ability of the circuit to block common-mode extrinsic noise was noted. This approach can significantly blunt large low-frequency common-mode noise, but, is compromised by the single-ended-to-differential conversion properties of the cross-coupled pair in differential VCOs.

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