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Noise and Spurious Tones Management Techniques for Multi-GHz RF-CMOS Frequency Synthesizers Operating in Large Mixed Analog-Digital SOCs

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This paper presents circuit techniques and power supply partitioning, filtering, and regulation methods aimed at reducing the phase noise and spurious tones in frequency synthesizers operating in large mixed analog-digital system-on-chip (SOC). The different noise and spur coupling mechanisms are presented together with solutions to minimize their impact on the overall PLL phase noise performance. Challenges specific to deep-submicron CMOS integration of multi-GHz PLLs are revealed, while new architectures that address these issues are presented. Layout techniques that help reducing the parasitic noise and spur coupling between digital and analog blocks are described. Combining system-level and circuit-level low noise design methods, low phase noise frequency synthesizers were achieved which are compatible with the demanding nowadays wireless communication standards.

1. INTRODUCTION

The major trend in nowadays wireless transceivers is towards single-chip CMOS integration. Designing low phase noise and low spurious tones frequency synthesizers that operate on the same die with a large and noisy digital core faces numerous system- and circuit-level challenges.

There exist two main mechanisms of parasitic noise and spurious tones coupling to the PLL building blocks: magnetic coupling and electric coupling. The magnetic coupling can appear between two bondwires, between a bondwire and the VCO or the VCO buffer on-chip spiral inductors, or between a bondwire and a metal interconnect line that creates a large magnetic loop. Electric coupling may appear either through the supply lines or via the substrate. Achieving a low phase noise PLL requires a good understanding of all these coupling mechanisms and adopting appropriate circuit- and system-level techniques that result in coupling minimization. A large mixed analog-digital SOC often has several digital supply bondwires that carry large current spikes which may couple to the bondwires providing the supply or signal to the sensitive PLL analog blocks. Increasing the distance between the aggressor bondwire and the receiving one, while ensuring a 90° orientation between them, is the most effective way to reduce the magnetic coupling. One example of critical magnetic coupling is between the bias bondwire of the voltage controlled oscillator (VCO) and any other aggressor bondwire, which may bring a significant variation of the local VCO supply. The nonlinear capacitance connected in parallel with the oscillator's LC tank determines a finite supply pushing gain. Thus the supply noise and spurs are upconverted around the carrier, degrading the VCO phase noise performance. To solve this issue, it has become a standard solution to bias the oscillator from a dedicated high PSRR regulator [1–4]. Another often encountered example is the coupling to the VCO control line in the applications that use an off-chip loop filter [5, 6]. Bringing the sensitive VCO control node off-chip is very dangerous since any magnetic coupling to the corresponding bondwire directly modulates the VCO frequency and thus results in spur and phase noise degradation. This is the main reason that on-chip PLL loop filters are always preferred.

Present design proposes a multiregulator PLL architecture for 802.11 a/b/g SOC applications, in which every single block from the PLL top level is biased from a dedicated series or shunt regulator. These regulators reduce both the impact of bondwire coupling and the parasitic noise and spur coupling between different PLL building blocks. If all analog and digital blocks are built in the same silicon substrate, a substantial noise coupling appears between them. To solve this

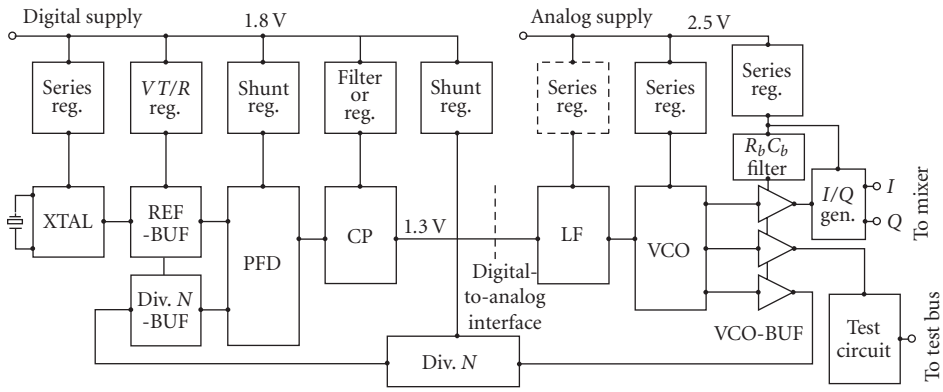

Figure 1: PLL top-level diagram including supply voltage partition and regulation.

troublesome issue, both the sensitive analog blocks and the noisy digital blocks were built in isolated substrates that are separated from the global chip substrate with deep N-well layers.

Modern deep-submicron CMOS processes often offer dual gate oxide thicknesses: thin gate oxide FETs that have a high operating frequency and a relatively low breakdown voltage and thick gate oxide FETs that have a medium operating frequency but a much larger breakdown voltage. Present design takes advantage of both device types to optimize the overall PLL phase noise performance.

The signal slew rate assumes very different values in the PLL building blocks (e.g., sinusoidal signal in XTAL oscillator and multi-GHz VCO and square-wave in the clock squaring buffers and the digital dividers). Therefore the impact that a given amount of supply noise has on these blocks can drastically differ. This paper presents a systematic design methodology to select the regulator type and architecture for each PLL building block.

The oscillator is the most sensitive analog block inside the PLL frequency synthesizer. Its tuning gain plays a crucial role in the PLL phase noise performance. The tuning gain needs to be high enough to cover the entire frequency range allocated to the given communication standard and also compensate for the process, temperature, and supply (PTV) frequency variations. The continuous shrinking of the supply voltage in modern deep-submicron CMOS processes, together with the progressive increase towards multi-GHz range of the operation frequency, has resulted in an ever high VCO tuning gain. A large VCO gain results in a degraded PLL phase noise due to a larger contribution of the PLL front-end stages noise and coupled spurious tones. A standard way to reduce the VCO gain is to break the frequency range into several subranges and use for each of them the entire tuning voltage range [3, 4, 7]. This paper proposes a high-resolution frequency calibration network to compensate for process variation, while a virtually constant varactor tuning gain is achieved by using several accumulation MOS varactors connected in parallel and having their $C(V)$ characteristics shifted one from the other, such that the individual gain peaks are distributed over the entire tuning range.

Power supply partitioning and filtering plays a key role in a low phase noise frequency synthesizer. Several low-voltage drop active RC filters are proposed to improve the PSRR of the headroom constrained PLL building blocks. For the cases when using only a filter or a regulator is not enough to provide the required PSRR, a cascade filter-regulator or a dual-regulator architecture was proposed. Most existing PLLs use one [5, 6, 8] or two [3, 9, 10] series regulators to bias the PLL building blocks. This paper presents a multiregulator PLL architecture together with a rigorous methodology to select the optimum regulator architecture for each PLL building block that minimizes the noise and spurious tones coupling when operating in a large mixed signal SOC.

2. PLL TOP LEVEL AND POWER SUPPLY PARTITIONING

Figure 1 presents the top-level diagram of the proposed low noise charge-pump PLL, including a crystal oscillator (XTAL) that provides a low phase noise sinusoidal reference clock to the PLL, a reference clock squaring buffer (REF-BUF) that converts the reference sine-wave into a square-wave, the phase-frequency detector (PFD) that compares the phase of the reference and feedback clocks and generates the up/down control signals for the charge-pump (CP), a loop filter (LF) that provides the loop stabilizing zero and reduces the ripple at the voltage controlled oscillator (VCO) control line, the VCO-BUF buffer that increases the edge speed of the multi-GHz output clock, the feedback divider (Div.N) that sets the reference frequency multiplication factor ($f_{\text{out}} = N^* f_{\text{ref}}$), and the divider buffer (Div.N-BUF) that drives the second input of the PFD. In addition to these main loop circuits, the PLL also has a quadrature clock generator (I/Q gen.) that performs a divide by two of the VCO output clock frequency and provides two clocks that are precisely at 90° phase difference, and a test circuit that brings at a test pin the signals at different analog and digital nodes from the PLL signal path for debugging purposes.

Investigating the PLL top-level diagram, one may identify two types of building blocks: digital circuits (PFD, Div.N, REF-BUF, VCO-BUF) and sensitive analog circuits (XTAL,

CP, LF, and VCO). Many large mixed analog-digital SOCs are pad-limited, allowing only a single supply (VDD, GND) for the entire PLL. When both the analog and digital PLL building blocks are biased from the same supply line, a particular care needs to be taken in order to avoid the noise and spur contamination of the global supply, which may result in noise coupling between the digital and analog circuits. In low phase noise PLLs it is sometimes critical to avoid also the coupling between two digital blocks. One such example is the noise coupling between the feedback divider (Div.N) that may generate tones that are not harmonically related to the reference frequency and the reference clock squaring buffer (REF-BUF) that can downconvert these tones into the PLL bandwidth, leading to high-level spurs.

Another situation encountered in many applications (presented in Figure 1) is when two supply lines are available to the PLL: one that biases the analog blocks and the second one that biases the noisy digital circuitry. In this case the designer needs to select the optimum boundary between the analog and digital power domains. The best choice for the analog-digital supply domain interface is at a high impedance node where the driving is done in current mode, as is the case for the charge-pump output node. Although the analog charge-pump is placed on the digital supply, using a current mode drive at the boundary between the two power domains, the noise between the analog and digital supplies is prevented from coupling into the signal path, as may be the case when the partition is done at a voltage-driven node (e.g., the up/down PFD output control signals).

The key target of the proposed low noise PLL power supply partitioning is to prevent parasitic noise and spur coupling between the analog and digital blocks. To achieve this, the sensitive analog circuits were biased from high forward PSRR series regulators, while the global supply contamination with digital switching noise was prevented by biasing the digital circuits with shunt regulators that provide a high value reverse PSRR. Starting from the PLL front end, the crystal oscillator does not generate significant supply current spikes. Its bias current is in fact held constant by the automatic amplitude control loop (AAC). Therefore the XTAL oscillator can be biased with a series regulator which does not provide any reverse PSRR rejection. The only reverse PSRR achieved by a series regulator is ensured by its load filtering capacitance. However, the noise and spurious tones reaching the XTAL oscillator and its output buffer (REF-BUF) can seriously degrade the PLL phase noise performance. Therefore a very low noise and high PSRR regulator is required. This paper proposes a novel dual-regulator architecture to bias both the XTAL oscillator and the VCO.

The reference and Div.N buffers dominate the in-band PLL phase noise. Their noise and spurs are directly magnified by the PLL gain ($= N$). It is therefore crucial to use a very low noise and high forward PSRR regulator for REF-BUF as well. Furthermore, the supply current spikes of the fast switching buffers do not need to be closed directly onto the global supply, since this may cause reference spur degradation through parasitic coupling to other sensitive PLL blocks (e.g., charge-pump and loop filter). A shunt regulator was used to ensure both a high forward and reverse PSRR rejection. Bandgap referenced regulators usually have a relatively large in-band noise, potentially degrading the REF-BUF phase noise performance through a modulation of its trip point. This design uses a very low noise V_T/R reference to generate the required PLL low noise reference currents and voltages.

The PFD has a much lower phase noise contribution due to the fact that its clock edges are very fast both at its input and also at its internal nodes. A high edge slope reduces linearly both the impact of the device internal noise and the supply injected noise. Therefore the usage of a regulator is not needed for the PFD from the forward PSRR point of view. However, due to the fact that the required supply voltage for the thin oxide gates (1.3 V) is smaller than the available system supply (2.5 V) and that it is preferable not to close the large current spikes of the fast switching digital gates onto the global supply, a second shunt regulator was used to bias the PFD.

For the charge-pump two contradicting requirements need to be satisfied. On one side, the voltage swing at the CP output needs to be as large as possible in order to reduce the VCO gain and thus decrease the noise and spur coupling from the PLL front end. This requires a high value supply voltage to the charge-pump. On the other side, minimizing the CP spurs downconversion mechanism due to its chopping action requires the usage of a well filtered or regulated local supply that reduces the effective supply voltage available to the CP. A regulator usually takes a much larger headroom in comparison with a simple RC filter ($2V_{\text{on}} + V_T$ for NFET output and V_{on} for PFET output). Therefore in this design an active RC filter was selected to improve the CP supply noise rejection.

The active loop filters are taking an almost constant supply current in lock conditions, allowing the usage of a series regulator to bias them [4, 11]. However, the presence of a supply line always comes with an elevated supply noise sensitivity. In the case of passive loop filters, there is no need for a regulator as they do not have a supply line. This paper presents a passive feedforward loop filter that significantly reduces the size of the on-chip loop filter capacitance, while requiring no supply line [12].

The VCO is the most sensitive analog block from the entire PLL design. Any supply noise or spur injection that reaches its local supply line is upconverted around the carrier by the supply voltage frequency pushing mechanism [13, 14]. It is now standard to bias the VCO from a dedicated high forward PSRR series regulator [1–4]. The VCO output buffer (VCO-BUF) which squares up the sine-wave looking clock generated by the oscillator leads to high amplitude supply current spikes due to the fast charging and discharging of the load capacitance. However, these current spikes are perfectly synchronous with the oscillator frequency and therefore cannot degrade VCO's phase noise. Hence it is not necessary to isolate the VCO-BUF from the clean analog supply with the help of a shunt regulator, as was done for the other digital blocks. However, the voltage level required by the VCO-BUF and the following I/Q generator that use thin gate oxide FETs is lower than the one used by the VCO (1.3 V

versus 1.5 V), requiring the usage of a separate series regulator. The VCO needs to operate at the maximum amplitude allowed by the device breakdown in order to minimize its phase noise. The device mismatches in the VCO-BUF may result in a significant pulse-width distortion of the resulting square-wave multi-GHz clock. This leads to a large second-order harmonic in the buffer supply current. If this second-order harmonic of the VCO frequency leaks to the I/Q generator, a large I/Q phase mismatch may result. A passive R_b, C_b filter was placed in series with the VCO-BUF supply line in order to close locally to ground its second-order harmonic current.

Finally, the feedback divider (Div.N) that generates most of the internal PLL switching noise is biased from a shunt regulator having a large reverse PSRR, which prevents the contamination of the global PLL supply with tones created by the divider switching. Analyzing the PLL top-level diagram presented in Figure 1, one may conclude that every single building block of the PLL signal path that needs a supply line uses an appropriate filter or regulator. The digital blocks are using shunt regulators that close locally their large supply current spikes, while the sensitive analog blocks use series regulators with large forward PSRR values to minimize the supply and spur injection.

Two supply voltages are available to the present SOC: 1.8 V used by the noisy digital core and 2.5 V used by the analog blocks in the signal path (LNA, mixers, VCOs). The frequency synthesizer uses two dedicated supply lines (see Figure 1). The PLL front end consisting of the digital building blocks (dividers, clock buffers, phase-frequency detector, and switched-current charge-pump) uses the 1.8 digital supply, since the clock edges are enough fast to be insensitive to the residual supply noise obtained after the high PSRR regulators. These digital blocks are built with thin gate oxide FETs that require a no larger than 1.3 V supply. Using a 1.8 V supply and high reverse PSRR shunt regulators results in a power efficiency level around 50%, but offers in return a good rejection of the supply noise and spurious tones.

It is important that the crystal oscillator and the reference clock squaring buffer are connected at the same ground line and there is no potential difference between their local grounds. Any noise voltage between the XTAL oscillator and its REF-BUF buffer may significantly degrade the reference clock phase noise since the slew rate of the input buffer signal (sine-wave) is rather low. A star connection of the two local grounds and a wide metal line (low series resistance) ensures that they are precisely at the same potential. However, biasing the sensitive XTAL oscillator from the noisy digital supply requires a very high PSRR dual-regulator architecture to avoid the supply spur degradation.

Separating the supply of the noisy digital building blocks from the sensitive oscillator prevents the contamination of the supply with reference frequency tones that may degrade the reference spur level. The front-end PLL regulators do not need a large bandwidth, since the noise and spurs coupled at the PLL input are strongly attenuated by the synthesizer lowpass-filter transfer function. This results in lower current levels in regulator's amplifier, improving its power efficiency. The shunt regulators used to bias the PFD and the PLL feedback divider have intrinsically a significantly lower power efficiency when compared to the series regulators. This is because their DC current needs to be larger than the average digital current in the worst-case process, temperature, and supply voltage corner. A digital calibration of the shunt regulator DC current based on the specific process corner and average die temperature lead to a power efficiency close to 50% even for the shunt regulators. The overall power efficiency of the PLL is around 45%.

The low phase noise reference XTAL oscillator and the output multi-GHz oscillator with their clock buffers need a more complex regulation scheme (two cascaded regulators or one regulator and a cascaded RC filter) to achieve the targeted noise and spur specifications. The XTAL oscillator amplitude is around 0.8 V, allowing the use of a dual regulator within a 1.8 V supply headroom. In contrast the output oscillator amplitude needs to be much larger (3 V peak-to-peak) to achieve a low phase noise, and therefore requires the use of the 2.5 V supply if a dual-regulator architecture is to be implemented. This lowers the power efficiency of the oscillator series regulator below the 50% level.

In an RF frequency synthesizer a lower power efficiency is always traded for better spur and phase noise performance. This gives one of the fundamental performance limitations for the portable application (battery operated) synthesizers. In wired applications the power efficiency is not that strongly constrained, and it is generally sacrificed to achieve a better synthesizer performance. The CMOS process scaling to 90 nm or 65 nm is accompanied by a supply voltage reduction (e.g., to 1 V), reducing the PLL power dissipation. The higher device f_T leads to faster clock edges and therefore a lower sensitivity to supply noise and spurious tones. This relaxes somewhat the specifications for the biasing regulators, further improving their power efficiency. However, the increase of the operating frequency in emerging wireless application up to 5 GHz, or in some cases beyond 10 GHz diminishes the power saving offered by the CMOS process scaling.

3. SUPPLY FILTERS

One solution to reduce the supply noise and spurious tones injection into the sensitive PLL blocks is to use a supply filter. Their advantages over a regulator are simplicity, smaller voltage drop, and lower die area. Figure 2(a) presents a standard passive RC filter. A first-order RC filter is shown, but higher-order filters can be also used for achieving a sharper frequency roll-off characteristic. In order to achieve an effective supply noise attenuation, it is required that the corner frequency of the filter is with at least one decade lower than the major supply noise frequency spectrum. Often the supply noise can have frequencies as low as few MHz, or even hundreds of KHz, forcing the RC filter corner frequency down to tens of KHz. The main drawback of the passive RC filter is that the DC current of the supplied block passes through the series resistor R_f. To prevent a severe reduction of the local supply voltage going to the PLL block, due to the supply current variation, a relatively low R_f value is needed. Usually the

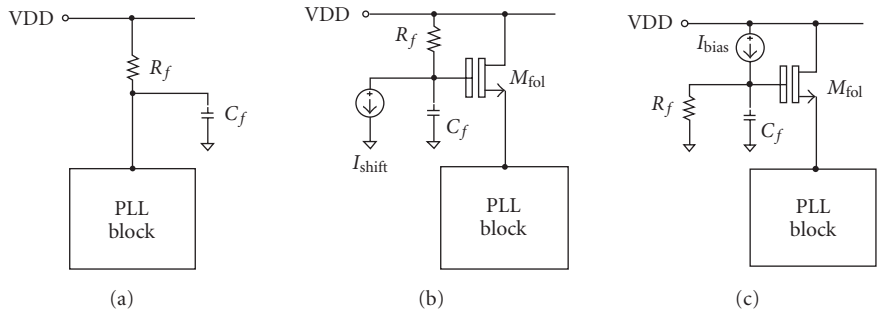

Figure 2: (a) Passive RC filter; (b) and (c) active RC filters.

tolerated voltage drop on R_f is only few hundred mV, resulting in a large C_f capacitance that can take a significant die area.

Active RC filters can be used to solve this problem [3, 4]. They consist as shown in Figure 2(b) of a low corner frequency R_f, C_f filter and an M_{fol} source follower. In this case the DC current of the PLL block does not go through the R_f resistor and therefore a large R_f value can be assumed. The supply current of the PLL block is provided by the M_{fol} active device that follows the filtered gate voltage as the local supply to the load block. The gate leakage of the M_{fol} follower is negligible, allowing for R_f a multi-MΩ value. The upper limit for R_f is set by the required noise level at the generated local supply. In circuits with high supply noise sensitivity this may be a stringent limiting factor (e.g., reference clock squaring buffer). The main drawback of the standard active RC filter is the large DC voltage drop equal to $V_T + V_{on}$ of the M_{fol} follower. The V_{on} component can be reduced by using a large W/L aspect ratio for M_{fol}. However, this increases its C_{gd} parasitic capacitance that in turn limits the high-frequency PSRR ($PSRR_{HF} = C_{gd}/(C_{gd} + C_f)$).

A more attractive implementation of the active RC filter can be achieved by using native (zero-V_T) NFETs [11]. In this case the voltage drop on the filter is only a V_{on} voltage that can be restricted to few hundred mV. Depending on the selected CMOS process, the threshold voltage of the native devices can be either slightly positive or slightly negative. If V_T is always higher than zero for all process and temperature corners, then the M_{fol} device is guaranteed to be in saturation region when diode-connected by the R_f resistor. However, if the threshold voltage can assume a negative value, then M_{fol} will be in triode region, preventing the supply noise filtering (M_{fol} is in fact a low value resistance that transfers the noise from the global supply line to the local PLL supply). To avoid the crashing of M_{fol}, a small I_{shift} current can be drawn out of the R_f, C_f filter, such that the V_{GD} voltage assumes an enough high negative value to prevent the triode mode operation of the M_{fol} follower. In many situations the large body effect on M_{fol} (their body is the global p-substrate of the die, which is connected to ground) may be enough to guarantee an always positive V_T for the native NFETs.

Using such an active RC filter built with a native NFET results in a very low-voltage drop (100–200 mV), while providing a PSRR in excess of 40 dB at medium and high frequencies. However, this circuit does not have any rejection at DC and frequencies lower than the R_f, C_f corner frequency. This may be an issue in the cases when DC-DC converters having significant spurs at tens of KHz are used to bias the SOC. Figure 2(c) presents an alternative architecture for the active RC filter that has a large supply rejection starting from DC. In this case the gate of M_{fol} is biased from a voltage achieved by injecting a bias current I_{bias} into an R_f, C_f filter. Its main drawback is that the output voltage is set by $I_{bias}{}^{*}R_f - V_{GS}(M_{fol})$ and does not track the global PLL supply. In some applications it is beneficial that the additional headroom available at higher supply voltages is provided as extra voltage range to the headroom constrained PLL blocks. However, this last active RC filter architecture is very useful in filtering the local supply to circuits that are sensitive to low-frequency supply noise (e.g., the oscillators).

4. BANDGAP AND V_T REFERENCE GENERATORS

Reducing the supply noise injection in a frequency synthesizer operating in a large mixed signal IC mandates the usage of a dedicated regulator for every single PLL building block. An isolation regulator can successfully reject the supply noise and spur injection, but it has noise of its own that may impact the VCO phase noise performance. Achieving a low noise regulator needs a low noise reference voltage generator. The most common way to generate a reference voltage is using a bandgap circuit [1–11]. Figure 3(a) shows a local bandgap voltage replica circuit that uses an $I_{bg} = V_{bg}/R$ current provided by the V-to-I converter of the master bandgap block that is injected into an R_{bg} resistor that closely matches the R resistor (in terms of unit resistor cells) used in the master bandgap circuit. Bandgap references have a good process and temperature stability, but come with a large output noise. The wideband noise can be filtered out with an RC filter, at the price of a large required die area due to the high value capacitance necessary to limit the total integrated white (thermal) noise to a low KT/C term. Rejecting the $1/f$ noise requires a very low corner frequency, which may not be feasible to implement on-chip. This design proposes an alternative way of achieving a low noise reference voltage using a V_T referenced circuit, as shown in Figure 3(b). The M_{ref} device provides the reference V_T voltage, which creates an $I_{ref} = V_T/R_{ref}$ current through the R_{ref} resistor. The M_{casc}

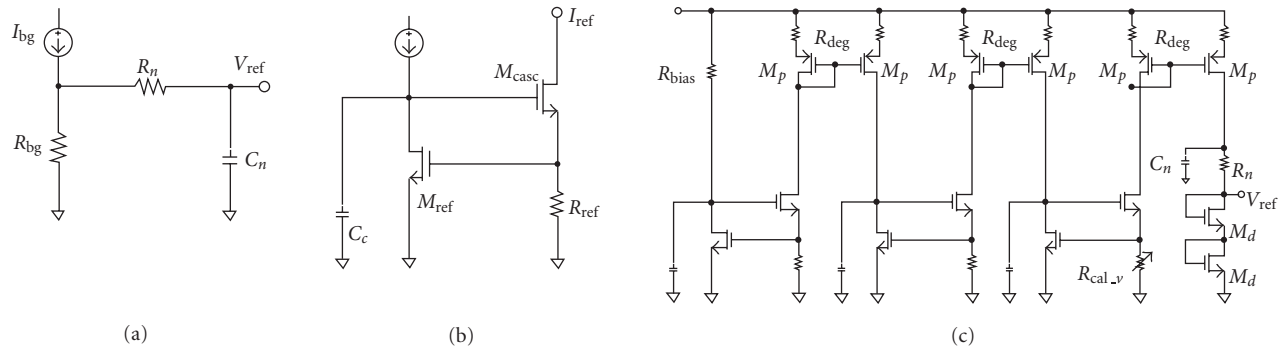

Figure 3: Reference circuits: (a) bandgap reference, (b) VT/R reference, and (c) improved PSRR VT/R reference.

cascode device boosts the output impedance of the current generator, helping to improve its PSRR. If enough loop gain is provided to the local feedback loop (M_{ref} and M_{casc}), the noise of the output current is dominated by the thermal noise of the R_{ref} resistor. Using a large degeneration resistor value reduces the reference current noise at the expense of a low current value. A reference voltage was generated by injecting the $I_{ref} = V_T/R_{ref}$ current into a low impedance load constituted by two diode-connected MOSFET devices (M_d) as shown in Figure 3(c). The V_T/R current generator can be biased using either an input current (I_{bias}) or a bias resistor (R_{bias}). For a given headroom voltage and current value the noise of a bias resistor is significantly lower than the one of a current mirror (e.g., $< 1\,\text{pA}/\sqrt{\text{Hz}}$ for a 20 KΩ resistor, versus about $6\,\text{pA}/\sqrt{\text{Hz}}$ for a 100 μA current source). However, using an R_{bias} resistor brings a strong supply voltage dependence of the input current ($I_{bias} = (V_{DD} - 2V_{GS})/R_{bias}$). This leads to a degraded PSRR of the current generator, increasing the sensitivity to supply noise injection. Three such V_T/R current cells were connected in cascade to improve the PSRR of the output reference voltage (see Figure 3(c)). Each V_T/R cell contributes at least 20–25 dB rejection of the input bias current supply dependence, resulting in an overall PSRR well in excess of 60 dB. The PSRR is no longer dominated by the input bias current, but is set by the resistive divider given by the output impedance of the turnaround PFET current mirror (M_p) and the low impedance of the diode-connected load devices (M_d). Resistive degeneration (R_{deg}) was used in the PFET current mirrors to reduce its noise contribution and improve the PSRR. The C_c compensation capacitance provides a dominant pole to the local feedback loop (M_{ref}, M_{casc}), ensuring a phase margin in excess of 60°.

The low noise performance of the V_T/R current generator comes at the price of a wide process and temperature variation. Optimizing the VCO phase noise performance requires the maximization of the oscillating amplitude, which in turns requires an accurate supply voltage level. A digital controlled resistor (R_{cal_v}) was used to calibrate the V_T referenced supply voltage (V_{reg}) to an accurate bandgap reference. To further reduce the noise and supply sensitivity of the output V_T/R reference current, a supplementary R_n, C_n noise filter was inserted in series with the output current leg.

5. SUPPLY REGULATORS

Active RC filters are generally recommended for low current blocks, when simplicity comes on the first place. The relatively large output impedance of the active RC filters ($1/g_m$) and also the increased voltage drop at large load currents due to an elevated V_{on} prevents their usage for biasing high supply current blocks. In these situations a regulator is more appropriate for reducing the supply noise injection. However, the regulator requires a larger voltage drop in comparison with a filter. One solution to achieve a high PSRR, while still using a moderate headroom, is using a cascade RC filter and series regulator as presented in Figure 4. The R_f, C_f, M_{fol} active filter helps improving the PSRR of the series regulator at high frequencies (above the regulator's bandwidth), where the PSRR drops sharply. At DC and low to medium frequencies (inside the regulator bandwidth) the active filter is not helping much, most of the PSRR being ensured by the regulator itself.

The series regulator uses a native (zero-V_T) NFET output device (M_{nreg}) to provide the high load current. Reducing the PSRR degradation caused by the $C_{gd}(M_{nreg})$ was achieved by using a PFET follower (M_{pfol}) that drives with a low impedance the gate of the output device. Its bulk needs to be connected at the source in order to avoid the substrate noise injection through the body effect. The M_{pfol} source follower helps also increasing the headroom available to the folding cascode current mirrors and allows the implementation of the C_c compensation capacitance with a lower area thin gate oxide NFET. A high gain amplifier is realized with a folded cascode NFET input differential pair (Min).

The reference voltage for the series regulator was generated with an $I_{bg} = V_{bg}/R$ current injected into a matched R_{bg} resistor. The C_{psrr} capacitor helps improving the PSRR of the reference voltage, while the R_n, C_n filter reduces the noise contribution of the local bandgap voltage generator (I_{bg}, R_{bg}).

Using a cascaded RC filter and regulator, a relatively high PSRR (> 50 dB) was achieved up to frequencies of tens of MHz. This is sufficiently high to reject the supply noise even in high bandwidth PLLs (several MHz). The cascade filter-regulator architecture can be applied to the noise sensitive

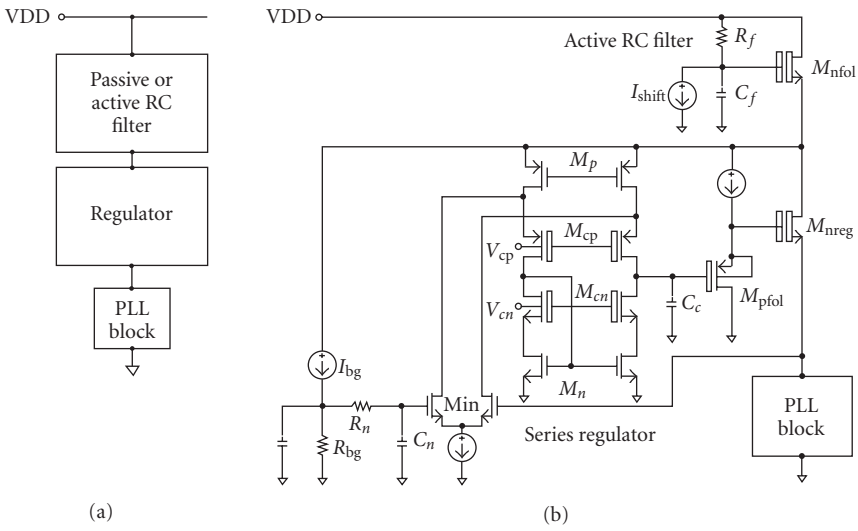

Figure 4: Cascaded filter and regulator: (a) principle; (b) implementation.

blocks from the PLL front end that have a lowpass or bandpass transfer function to the output clock phase noise.

In high-frequency VCOs the percentage of the tank capacitance coming from the nonlinear device parasitic capacitance is large, leading to a higher supply pushing gain (K_{vdd}) in comparison with the low-frequency VCOs, where most of the tank capacitance is contributed by the linear MIM or metal capacitors. Furthermore, in large mixed signal SOCs the supply voltage is highly contaminated with spurious tones coupled both magnetically and electrically from the switching digital circuits. Using an off-chip filtered supply dedicated only to the low noise oscillator eliminates the board-level noise coupling, but it does not solve the supply noise injection through magnetic coupling between the different IC bondwires. On-chip filtering usually requires a very large die area. Increasing the distance between the sensitive analog pads and the aggressor digital pads and using a 90° orientation between the corresponding bondwires helps reducing the coupling. Flip-chip assemblies can be also used to avoid the bondwire coupling, but at a significant cost increase penalty.

Multi-GHz VCOs have intrinsic supply pushing gains of several MHz/V. Bandgap references come with noise levels around few hundred nV/$\sqrt{}$Hz. The resulting supply noise injection limits the VCO phase noise to less than 80 dBc/Hz at 100 KHz frequency offset, value that is not acceptable for many modern communication applications. Achieving less than −100 dBc/Hz VCO phase noise at 100 KHz offset requires a supply noise no higher than few tens of nV/$\sqrt{}$Hz and a supply pushing gain of only few hundreds of KHz/V. In the present application, tolerating a broadband 100 mV peak-to-peak supply voltage ripple with a 100 KHz/V supply pushing gain (after supply pushing cancellation) requires a minimum 65 dB PSRR at 1 MHz and in excess of −45 dB PSRR at 10 MHz to achieve the −80 dBc supply injected spur level.

Most existing VCOs use a single regulator to minimize the phase noise degradation due to supply injected noise and spurious tones [3, 5, 10–12]. The oscillator is usually placed inside a phase-locked loop to generate a stable output clock frequency. The PLL feedback loop highpass filters the noise and spurious tones of the oscillator. The corner frequency of the transfer function is PLL's natural frequency (f_n). At frequencies lower than f_n the loop attenuates oscillator's phase noise, while for frequencies higher than f_n the feedback loop is inactive (open), letting the output clock phase noise follow the VCO phase noise characteristic. Achieving a low supply injected noise and spurs requires a high regulator PSRR up to at least one decade above the PLL's natural frequency (typical up to several MHz, or few tens of MHz). Achieving a large PSRR value at high frequencies requires a large regulator bandwidth, which increases its output voltage noise due both to the reference voltage and the regulator amplifier contributions. This results in a significant degradation of the VCO phase noise through the supply pushing mechanism which upconverts the low-frequency noise of the regulator into phase noise skirts around the multi-GHz carrier. Particularly troublesome is the $1/f$ noise of the regulator. Once $1/f$ noise is created, it is hard to filter, since it requires very large R and C values, which are hard to integrate on-chip. The preference is to use a regulator with low $1/f$ noise to begin with. Usually the PLL bandwidth is selected to be much larger than the VCO's $1/f^3$ phase noise corner frequency, such that the $1/f$ noise upconversion has a small impact on the PLL output integrated phase noise. Strong resistor degeneration was used in the regulator reference voltage circuit to minimize the active device $1/f$ noise contribution (R_{deg} in Figure 3(c)).

A large regulator bandwidth as required by a high PSRR value comes in contradiction with the regulator's low noise requirement. This paper uses a dual-regulator architecture to bias the VCO [15]. Using two cascaded regulators solves the contradiction between PSRR and noise requirements by distributing the two specifications over the two regulators. Figure 5(a) presents the principle diagram of the dual-regulator architecture. It consists of a first wide-bandwidth

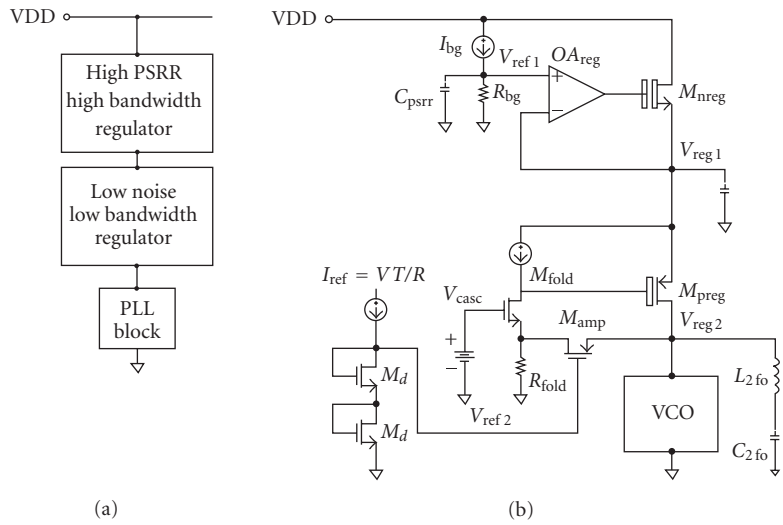

Figure 5: Dual regulator: (a) principle; (b) implementation.

regulator that provides a large value PSRR up to high frequencies, followed by a second narrow-bandwidth regulator that provides the low noise output voltage. Since the noise requirements of the first regulator are relaxed, a standard bandgap voltage reference can be used, as shown in Figure 3(a). In contrast, the second regulator needs to use a very low noise reference voltage, achieved by using a V_T reference circuit as shown in Figure 3(c). The degraded PSRR of the second regulator at high frequencies is not a concern, since most of the overall PSRR performance of the dual-regulator architecture is ensured by the first wide-bandwidth regulator. Distributing the challenging noise and PSRR specifications between the two regulators results in a PSRR in excess of 60 dB up to tens of MHz, while the output voltage spot white noise is lower than 20 nV/$\sqrt{}$Hz.

Figure 5(b) shows the detailed schematic of the dual VCO regulator. Standard V_T NFETs cannot be used as series devices due to the large resulting voltage drop on the regulator, which leads to a reduced amplitude in the oscillator, with detrimental effect on the phase noise performance. A PFET output device will significantly degrade the PSRR of the first wideband regulator, particularly at medium and high frequencies. To solve the large voltage drop issue of the NFET series regulators, while simultaneously achieving a high PSRR, the first wideband regulator was implemented with a zero-V_T (native) NFET device, which comes at no extra cost in the selected CMOS process.

The bandgap reference voltage for the first regulator was generated by injecting an I_{bg} current into an R_{bg} resistor. The C_{psrr} capacitor improves the PSRR of the reference voltage at high frequencies when the supply noise propagates directly through the capacitor divider given by the C_{gd} parasitic capacitance of the I_{bg} current mirror and the C_{psrr} filtering capacitance.

The second narrow-bandwidth regulator uses a single-ended amplifier implemented with the M_{amp} common-gate stage, followed by the M_{fold} folding cascode stage. It minimizes the noise of the regulator, while ensuring a large feedback loop gain value. A differential amplifier leads to a larger intrinsic noise when compared with a single-ended implementation, for the same loop gain value. The supply voltage for the oscillator is given by $V_{SG}(M_{amp})$ and $V_{GS}(M_d)$. A digital calibration of the V_T/R reference current was used to achieve a tight control on VCO's local supply voltage, allowing its amplitude maximization.

The mismatches in the clock path differential buffer create second-order distortion terms. If the second harmonic leaks to the oscillator a further degradation of its phase noise may happen [24]. To avoid this, a high quality factor series LC circuit tuned at the second harmonic of the highest oscillator operating frequency was placed in parallel with the oscillator. In the considered process the highest Q is achieved by the MIM capacitors and the bondwire inductors. Achieving a large rejection factor was possible by using a $C_{2\,fo}$ MIM capacitor connected in series with an $L_{2\,fo}$ bondwire connected to the package paddle, constituting the ground plane. At lower operating frequencies the $L_{2\,fo}$, $C_{2\,fo}$ circuit shows less attenuation of the second harmonic, but the VCO phase noise is also lower.

6. CRYSTAL OSCILLATOR

The main role of a crystal oscillator is to generate a low phase noise sinusoidal reference clock for the PLL. The operating frequencies of low-end XTALs are limited to 20–40 MHz due to their fundamental tone operation. Overtone crystals can go as high as few hundred MHz, but at a large cost increase. The PLL front-end noise is amplified by the feedback divider modulus (N). In multi-GHz frequency synthesizers the gain can be as high as 40–60 dB, resulting in a large magnification of the reference clock path phase noise. For this reason, it is preferred to use the XTAL with the highest available frequency within the targeted cost range.

Historically, most of the XTAL oscillators are realized with Pierce configuration (common source amplifier) as shown in Figure 6(a) [3–6]. The main advantage of this

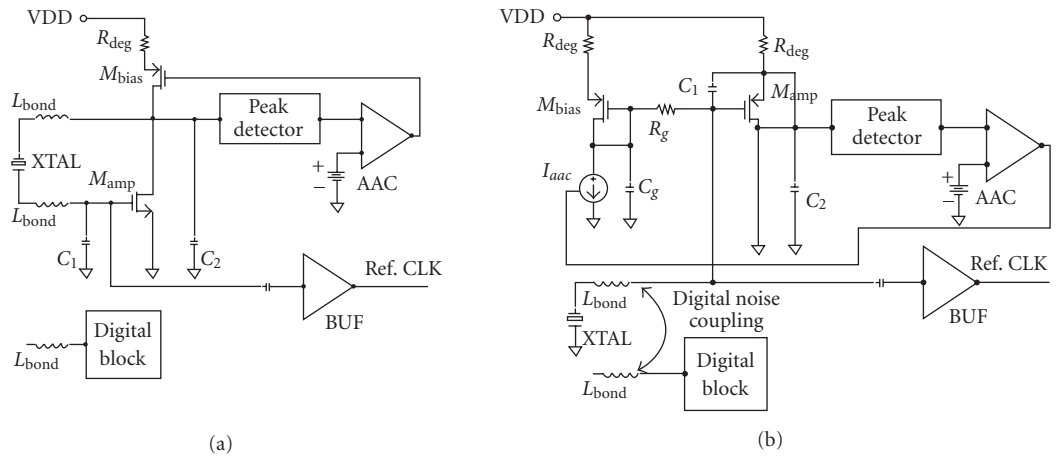

Figure 6: XTAL oscillators: (a) Pierce configuration, (b) Colpitts configuration.

architecture is that the two tank capacitors C_1 and C_2 are grounded and can be implemented with MOS capacitors, resulting in a relatively low die area. The bias current for the M_{amp} amplifier is generated by a resistive degenerated (R_{deg}) PFET current source (M_{bias}) controlled by the automatic amplitude control loop (AAC). Another advantage of the Pierce configuration is the class C operation of the M_{amp} device that is ON only at the peak positive amplitude of the generated sine-wave, when the phase noise impulse sensitivity function is at a minimum [13]. This results in a very low phase noise contribution coming from the M_{amp} device. The XTAL oscillator phase noise is dominated by the crystal tank losses and the bias current source driven by the AAC loop that are always ON (operated in class A).

A standard analog AAC loop consists of a peak detector, a reference voltage generator, and an AAC loop amplifier/comparator [16, 17]. Lower AAC loop phase noise contribution was achieved with a digital implementation in which the output of the peak detector is converted to digital domain by an ADC and the loop amplifier is replaced by a noiseless digital state machine that controls the bias current via a current DAC [18].

The most significant XTAL noise contribution to the PLL output clock phase noise is at low-frequency offsets from the carrier, where the $1/f$ noise upconversion of the active devices dominates [13, 14]. Therefore from the multitude of Pierce oscillator configurations the lowest phase noise is achieved by the one using an NFET amplifier operated in class C and a PFET bias current source operated in class A (see Figure 6(a)). The justification resides in the much lower $1/f$ noise of the deep-submicron PFETs (an order of magnitude lower) in comparison with the NFETs.

Implementing the C_1 and C_2 capacitors off-chip is a bad choice in the case of large mixed analog-digital SOCs. This is because the XTAL bondwires may magnetically couple large spurs from the biasing bondwires of the digital circuits which carry high amplitude current spikes. The coupled voltage is divided between C_1 or C_2 capacitors and the M_{amp} parasitic capacitances. As the last ones are usually much lower in comparison with C_1 and C_2, most of the magnetically coupled voltage appears at the gate of M_{amp} and therefore at the input of the reference clock squaring buffer (REF-BUF).

The XTAL oscillator generates a sinusoidal signal, while the PLL requires a square-wave clock. A squaring buffer is usually used to accomplish the edge squaring operation. The nonlinear edge squaring performed by REF-BUF buffer is in fact a phase sampling action that results in high-frequency noise and spurs aliasing down into an f_{ref} interval around the XTAL carrier. Thus the squaring buffer is capable of down-converting into the PLL bandwidth the high-frequency noise and spurs that reach the buffer input. Reducing the amplitude of the coupled spurs at the input of the squaring buffer requires an on-chip implementation of the C_1 and C_2 capacitors. In this case the bondwire coupled voltage is heavily attenuated by the capacitive divider formed with the parasitic pin and pad capacitance added with the PCB capacitance on one side and the on-chip C_1/C_2 capacitors and the amplifier parasitic capacitance on the other side.

From the phase noise perspective using an NFET amplifier is a major drawback for a Pierce oscillator. Furthermore, it requires two bonding pads to connect the crystal, being ill-suited for pad-limited SOC applications. Figure 6(b) presents an alternative way to implement a crystal oscillator using a Colpitts configuration (common drain amplifier). A PFET amplifier M_{amp} is used in order to reduce the $1/f$ noise impact, while a resistively degenerated (R_{deg}) current mirror (M_{bias}) was used to bias the amplifier. The common-mode voltage at the gate of M_{amp} was chosen close to the supply voltage, such that a class C operation can be achieved, with its dramatic phase noise improvement impact. Moreover, the crystal requires only a single connecting bondwire (L_{bond}), being advantageous for pad-limited SOCs. An R_g, C_g filter was used to minimize the noise contribution of the M_{bias} device. The main drawback of the Colpitts common-drain configuration is the requirement of a floating capacitance (C_1) that needs to be implemented either as a MIM or as a metal interconnect capacitance. Therefore it requires a larger die area in comparison with a MOS capacitor. The last ones cannot be used as floating capacitor since their large bottom plate parasitic capacitance gives a high substrate noise

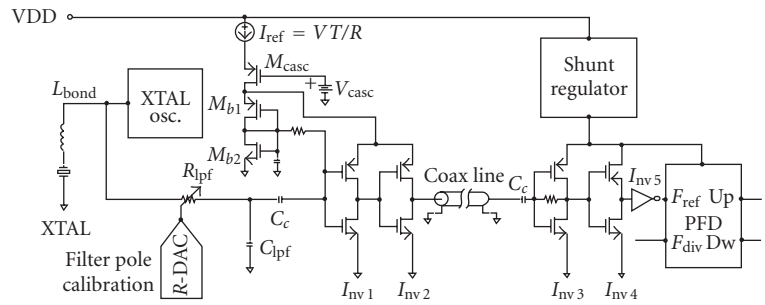

Figure 7: Low noise and low coupled spurs reference clock signal path.

injection. The larger die area taken by the Colpitts XTAL is offset by the much lower phase noise in comparison with a Pierce configuration. This results both from a larger oscillation amplitude allowed by a common drain amplifier (only one device versus two stacked devices in the Pierce oscillator) and the reduced contribution of the M_{bias} noise to the oscillator phase noise.

Another important design choice is the type of FET devices (thin or thick gate oxide FETs) used for both the amplifier and the AAC loop. The thick gate *I/O* devices can hold a larger voltage (2.5 to 3.3 V), resulting in a larger amplitude with a quadratic impact on the phase noise [13]. Thin oxide FETs can withstand only a 1 to 1.3 V voltage, drastically limiting the oscillator amplitude. However, they have a significantly lower $1/f$ noise (direct proportional with T_{ox} oxide thickness), which results in a much lower $1/f^3$ phase noise.

The spurs coupled to the XTAL local supply are translated near the XTAL carrier through the crystal oscillator supply pushing resulted from the nonlinear capacitance connected in parallel with the crystal [14]. Any spur that appears on the reference clock path is amplified by the large PLL closed-loop gain (equal to the N modulus value inside the loop bandwidth), often resulting as the dominant spur mechanism in the PLL. A dual-regulator architecture was used to achieve a PSRR in excess of 60 dB up to high frequencies (at least one decade above the PLL natural frequency). With 0.5 V voltage drop on each regulator and a 2.5 V global supply, the local supply of the XTAL oscillator comes close to the breakdown voltage of the thin oxide FETs. Therefore both the amplifier with its bias current source and the AAC loop peak detector and amplitude comparator were implemented with thin oxide FETs, benefiting of their much lower $1/f$ noise.

7. REFERENCE CLOCK PATH

For a low noise PLL it is crucial to achieve a low phase noise edge squaring operation. This is performed by the reference clock buffer presented in Figure 7. As mentioned before, this nonlinear operation is capable of downconverting the high-frequency noise and spurious tones from both the squaring buffer input and its supply line, directly inside the PLL loop bandwidth, where no rejection is presented. This mechanism is particularly dangerous in large bandwidth PLLs when the chance of getting a spur inside the loop bandwidth is much higher. Furthermore, large SOCs pose supplementary challenges when they have multiple clock domains that are not harmonically related, opening the path to spur down-conversion due to the nonlinear functions existent in the signal path.

One of the dominant spur coupling mechanisms at the squaring buffer input is through the crystal bondwire. To minimize the spur that arrives at the input of the squaring buffer, an RC lowpass filter (R_{lpf}, C_{lpf}) was placed between the L_{bond} bondwire and the input of REF-BUF. This attenuates the high-frequency spurious tones before they are applied to the nonlinear edge squaring operation with down-conversion capability. To avoid phase noise degradation due to reference clock slewing (which generates noise aliasing), the RC filter should have its corner frequency higher than the PLL reference frequency. Ensuring this condition over all process and temperature corners results in a larger typical corner frequency and thus a lower attenuation of the high-frequency spurs. A maximum attenuation can be achieved by using the lowest possible corner frequency in the RC filter. This design uses a calibrated RC filter that has a resistor DAC to adjust the RC filter time constant, such that its corner frequency stays constant over all process corners and is positioned with one octave above f_{ref}. The maximum R_{lpf} resistance is determined by its own noise contribution to the overall PLL phase noise. On the other side, a too low R_{lpf} resistance results in a very large C_{lpf} capacitance that may heavily load the crystal tank, potentially reducing its quality factor and thus increasing the XTAL oscillator phase noise.

To avoid large pulse-width distortion in the reference clock path due to differences between XTAL oscillator and squaring buffer common-mode levels, an AC coupling through the C_c capacitor was used. The DC bias voltage to the input of the squaring buffer is provided by two replica diode devices M_{b1}, M_{b2} and an isolation RC filter. The supply voltage for the front-end inverters of the squaring buffer ($I_{nv\,1}$ and $I_{nv\,2}$) is provided by an open-loop shunt regulator built with a low noise $I_{ref} = V_T/R$ current injected into the M_{b1}, M_{b2} replica diode-connected devices. This circuit provides a high forward PSRR to minimize the supply noise and spur injection into the local buffer supply. Changes in the local supply modulate the inverter trip point and thus create jitter. To further improve the PSRR of the shunt regulator, the gate of the M_{casc} cascode device is referenced to

ground via a V_{casc} voltage source, as opposed to the supply referencing used by a standard cascode current mirror, which has a degraded PSRR due to the direct supply noise injection through the $C_{\text{gd}}(M_{\text{casc}})$ parasitic capacitance. The shunt regulator offers also a large reverse PSRR which is important for minimizing the reference spur contamination of the global PLL supply due to the large current spikes generated by the fast switching squaring buffer inverters. The reference frequency modulation of the supply given by its effective impedance (set with the on-chip bypass capacitance and the supply bondwire inductance) may couple to other sensitive analog blocks (e.g., loop filter or VCO) and thus degrade the PLL reference spur performance. In present design, for a 50 ps 10-to-90% rise/fall time and a 1.2 V supply the slew rate is 20 GV/s. For such fast reference clock edges a PSRR of only −40 dB is required from the corresponding shunt regulator to achieve output spurs lower than −80 dBc, when the PLL gain is 50 dB and the supply voltage ripple is 100 mV peak-to-peak.

Once the reference clock edges are squared up (have a high slew rate), it is important not to slow them down again before reaching the PFD, since this may create a second noise aliasing point in the reference clock path at the point where the edges are squared up a second time and thus degrade the reference clock phase noise. The first stages of the squaring buffer ($I_{\text{nv}1}$ and $I_{\text{nv}2}$) need a very low noise supply voltage. Bandgap references are often used to generate supply voltages [1–11]. However, they are notorious for their high noise level which disqualifies them for the reference clock path bias generator. A V_T/R reference current was used instead (see Figure 3(b)) that has a much lower $1/f$ and thermal noise due to a large degeneration resistor (R_{ref}). Injecting a low noise $I_{\text{ref}} = V_T/R$ current into low impedance diode-connected FETs, a very low noise supply voltage is achieved. The large process and temperature variation of this voltage is not an issue for the REF-BUF since it tracks the trip point of the squaring buffer inverters.

The internal phase noise of the squaring buffer is dependent on the noise contributed by the NFET and PFET of the first inverter ($I_{\text{nv}1}$) around its trip point, where the edge position is decided. Using a low supply voltage equal to $V_{Tp} + V_{Tn}$ for the squaring buffer allows only one device to be in strong inversion around the trip point (either the NFET or the PFET). Since the two devices cannot be simultaneously in strong inversion (as is the case for a standard inverter biased from an elevated supply voltage), the phase noise of the squaring buffer is significantly reduced. Using only one device to drive the load capacitance reduces somewhat the edge speed, but the much lower device noise offsets by a large amount the higher noise to phase noise conversion gain due to the lower edge slope.

The PFD is usually operated at the nominal thin gate oxide FET supply voltage (e.g., 1.3 V in a 0.13 μm CMOS process). Therefore it was biased from a separate closed-loop shunt regulator. A second pair of capacitive coupled inverters ($I_{\text{nv}3}$ and $I_{\text{nv}4}$) was used to perform the level shifting of the reference clock digital levels and also provide the additional required drive strength. In most crystal oscillators the phase noise of the rising and falling edges are not identical. For example, in the Pierce oscillator case (Figure 6(a)) the rising edge at the M_{amp} drain has a lower phase noise since the M_{bias} PFET with lower $1/f$ noise is driving the edge. The falling edge is noisier due to the higher $1/f$ noise of the M_{amp} NFET that is driving the edge. For a low noise PLL it is important to select the lower phase noise edge to drive the PFD. A similar situation happens in the Colpitts XTAL oscillator (Figure 6(b)) where the rising edge in the source of M_{amp} has lower phase noise. Therefore the Pierce oscillator requires a even number of inverters between the gate of M_{amp} and the input of the PFD (assuming the PFD is falling edge sensitive), while the Colpitts oscillator needs an odd number of inverters. If the XTAL oscillator (usually placed in the pad ring) and the PFD are not in close proximity, a coaxial metal shield needs to be used for the reference clock path in order to avoid parasitic coupling to the clean reference signal.

8. PHASE-FREQUENCY DETECTOR

The PFD compares the phases of the reference and feedback clocks and generates the up/down digital control signals for the charge-pump. Both its input clocks and the internal node signals are square-waves with high edge slew rate, which minimizes the PFD phase noise contribution (both from internal device noise and the supply injected noise). Minimizing the phase noise contribution of the charge-pump current sources requires the reduction of the time interval that both currents are ON during each reference clock cycle. This also decreases the amount of supply noise and spurious tones that are downconverted by the charge-pump chopping action. To achieve this goal, the PFD needs to have a very fast reset signal propagation time, which requires a minimal number of logic gates in the PFD signal path and also the usage of the fast thin gate oxide FETs.

PLLs that use source, gate, or drain switch charge-pump architectures have a relatively slow switching time (few nanoseconds) and therefore require wide up/down PFD pulses to ensure that the charge-pump current sources are active when the phase difference measurement is performed. If the PFD control pulses are narrower than the CP switching time, the so-called dead-zone appears in the PFD-CP transfer function, since the CP does not have enough time to fully switch and thus correct for the phase difference measured by the PFD. The dead-zone in the charge-pump transfer function can seriously degrade the PLL jitter performance, since during this time interval the feedback loop is opened and the clock edges are moving randomly till they generate a phase difference enough large to bring the charge-pump out of the dead zone region. The seven-NAND implementation of the dual D-flip-flop PFD is very popular in CMOS PLLs [1–6]. However, it has a large reset time equal to seven gate propagation times, which typically ranges between 300 pioseconds and 1 nanoseconds depending on the device type and sizes. If a larger reset time is required (several nanoseconds), additional inverters can be introduced in the reset signal path [3].

If the CP transfer function is dead-zone-free, then the PLL reference spurs are reduced linearly with the decrease

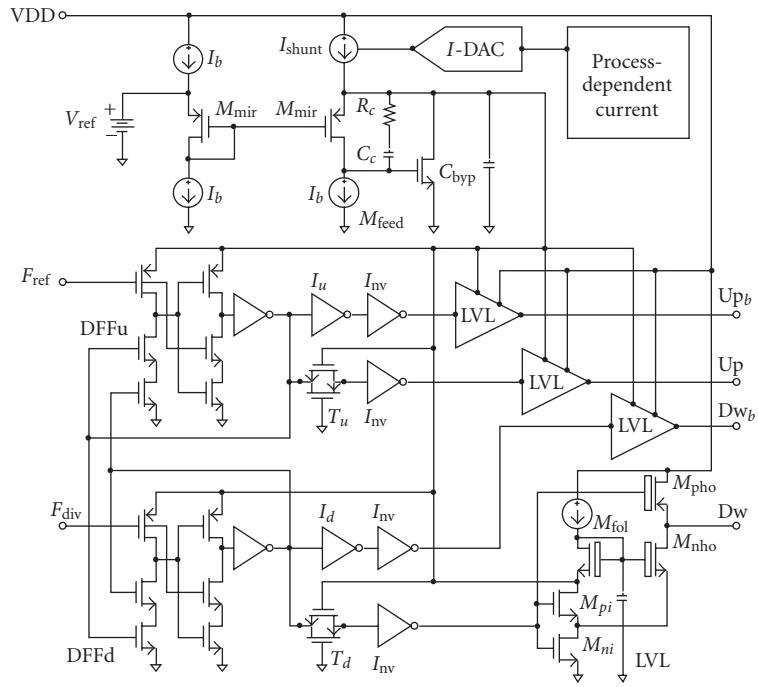

Figure 8: Phase-frequency detector (PFD) with dedicated shunt regulator.

of the CP pump-up and pump-down pulse widths. The limit to which these pulses can be reduced is set by the CP switching speed. The selected differential current-steering CP architecture provides worst-case switching times as low as 50 pioseconds in 0.13 μ CMOS. A PFD reset time as low as 100–150 pioseconds was achieved by using thin gate oxide FET dynamic D-flip-flops as shown in Figure 8 [4]. They result in only three gate delays in the reset signal path. The PFD feedback NAND gate that generates the reset signal for the two flip-flops was built within the dynamic flip-flop structure by using the $M_{\text{rst}\,1}$ and $M_{\text{rst}\,2}$ devices. This reduces by one gate delay time the minimum up/down pulse width when the PLL is in lock condition.

The PFD generates single ended up/down signals, while the differential current steering charge-pump requires also the complementary upb/dwb signals. These last ones are generated by adding a parallel path at PFD output, having one more inverter in comparison with the main up/dw signal path. Reducing the glitch current created by the charge-pump switching requires a good synchronization of the up/dw and upb/dwb signals. To achieve this, two always-ON transmission gates T_u/T_d were added in the up/dw signal paths to match the propagation time through the extra inverters (I_u/I_d) from the complementary upb/dwb signal paths. Reducing the current glitch in the charge-pump requires keeping the common-mode voltage at the NFET differential current steering pair high and the common-mode at the PFET differential current steering pair low, such that at all times there is at least one device in each differential pair that is ON. If at a given moment both devices of the differential current steering pair are turned off due to an un-appropriate common-mode level, a large charge-pump current spike is generated, which may result in significant VCO control voltage ripple and thus a serious PLL reference spur-level degradation.

To achieve a fast reset in the PFD, thin oxide FETs were used, while a low supply voltage (e.g., 1.3 V) was provided in order to avoid device breakdown. In contrast, the charge-pump uses the highest supply voltage available in the system, such that a large oscillator control voltage swing is ensured, as required by a low VCO gain. A level shifter stage need to be introduced between the PFD and the charge-pump, that performs the appropriate digital signal logic-level conversion. Positive feedback cross-coupled differential inverters are often used to perform the level shifting function [1]. Their main drawback is the lower edge speed due to the large gate capacitance of the cross-coupled devices that loads heavily the signal path. Furthermore, positive feedback circuits are notorious for their degraded phase noise and therefore they should be avoided in the low phase noise PLL front end. This design proposes a new level shifter architecture shown in Figure 8 that achieves a much higher edge speed in comparison with the cross-coupled architecture, without using the positive feedback to regenerate the logic level to the higher supply. It consists of a low voltage thin gate oxide inverter M_{ni}/M_{pi} and a protection high-voltage thick gate oxide current mirror $M_{\text{fol}}/M_{\text{nho}}$. For an output Low state the M_{ni} device is pulling down and the M_{nho} device operates in triode region, propagating the Low state to the output. The fast thin oxide NFET guarantees a rapid discharge of the load capacitance and therefore a short fall time. For a logic High at the output, the input is in the Low state. Therefore a high voltage thick oxide PFET M_{pho} can be used to pull-up the output node. A proper sizing of this output PFET is required

to provide a balanced rise/fall time at the level shifter output. The input capacitance of the level shifter is given by the thin oxide inverter and the gate capacitance of the thick oxide pull-up PFET. The last inverter layer in the up/dw/upb/dwb signal paths need to be designed to drive this larger input capacitance of the level shifter, while the level shifter needs to be strong enough to be able to drive safely the input capacitance of the charge-pump switches. The switches size is dictated by the $1/f$ noise of the differential current steering pair, which sets the W/L aspect ratio for the differential pair devices.

Generating fast edges in the PFD and in its output level shifter requires large supply current spikes that may degrade the PLL reference spur performance if they leak to the sensitive analog blocks (e.g., loop filter or VCO). Preventing the reference ripple coupling through the PLL global supply is ensured by biasing the PFD and its input and output level shifters from a separate shunt regulator that has a large reverse PSRR. An open-loop shunt regulator cannot be used in this case due to its relatively large output impedance that would create a large local supply ripple as a response to the high amplitude supply current spikes. A closed-loop shunt regulator was used instead as presented in Figure 8 [19]. The reference voltage V_{ref} is followed at the output through the M_{mir} PFET current mirror that is kept always active by the I_b bias current sources. The shunt regulator presents to the global PLL supply line a constant I_{shunt} current load. This current either provides the large supply current spikes of the digital circuitry, or it is dumped to ground by the M_{feed} local feedback device. An R_c, C_c compensation circuit is used to guarantee a good phase margin of the local feedback loop constituted by M_{mir} and M_{feed}.

A local bypass capacitance C_{byp} was added to provide the high-frequency component of the digital load current, while the low- and medium-frequency current components (up to the local feedback loop bandwidth) are provided by the shunt regulator. To guarantee a high reverse PSRR, it is necessary to design the I_{shunt} DC current to be larger than the highest DC component of the digital circuitry supply current over process, temperature, and supply corners (PTV). The digital circuit presents a very wide range supply current variation over PTV requiring an over-designed I_{shunt} current. To avoid current wasting in the shunt regulator, the I_{Shunt} current was set by a current DAC (I-DAC) controlled with a circuit that tracks the process corner of the thin gate oxide FETs, which constitute most of the digital circuitry load capacitance.

9. CHARGE-PUMP

The charge-pump (CP) is a key block for a low noise and low spur-level frequency synthesizer. In lock conditions the CP current sources are turned-on for a very short period of time, being OFF for most of the reference clock cycle. Therefore the intrinsic noise of the CP is multiplied in time domain with a periodic rectangular switching function. This corresponds to a convolution in the frequency domain with a discrete sinc spectrum, having the spacing between the tones equal to the reference frequency, while the main lobe width is equal to twice the inverse of the CP on-state time. The $1/f$ noise of the charge-pump currents has usually a low corner frequency (few MHz down to hundreds of KHz) which is much lower than the PLL reference frequency (tens of MHz). Therefore the switching action of the charge-pump does not result in aliasing of the $1/f$ noise. The PLL closed-loop transfer function has a lowpass shape with the corner frequency at the PLL loop natural frequency ($\approx$ 0.5 MHz). Therefore at the output of the PLL appears only one lobe of the CP $1/f$ noise spectrum. The $1/f$ noise power spectrum is attenuated by the square of the switching waveform duty cycle. Hence the CP $1/f$ noise current (A/$\sqrt{\text{Hz}}$) is effectively scaled down by the duty cycle of the switching waveform.

The charge-pump white noise undergoes aliasing in the frequency domain due to its wide bandwidth spectrum. After piling up the different aliased white noise components (coming from the convolution with each discrete tone from the switching waveform spectrum), they are lowpass filtered by the PLL closed-loop transfer function. As a consequence, the aliasing effect diminishes the noise reduction brought by the switching waveform duty cycle. The noise power is reduced linearly with the duty-cycle, while the equivalent CP output white noise current is reduced by the square root of the duty cycle value. Summarizing, both the $1/f$ and the white noise originated in the charge-pump can be reduced by minimizing the time interval that the CP is ON (low duty cycle of the switching waveform).

Besides reducing the duty cycle, a second way to reduce CP noise contribution is to minimize its intrinsic noise. The charge-pump is in essence realized by two complementary current mirrors connected to the PLL loop filter high impedance node. In a current mirror both the input (master) and the output (slave) devices contribute noise. If the noise of the output devices M_{no}/M_{po} is unavoidable, the noise of the input devices M_{ni}/M_{pi} can be filtered-out by using two very low corner frequency RC filters (R_n, C_n) as shown in Figure 9. To provide an effective noise filtering, the corner frequency of the R_n, C_n lowpass filter needs to be at least one decade lower than the PLL natural frequency. The value of the R_n resistor is limited by its own white noise contribution. Therefore large on-chip C_n capacitors are usually required by the CP noise filters.

Large-area deep-submicron FET filtering capacitors (thousands of μm^2) come with relatively large gate leakage currents (μA at the maximum IC temperature), which in conjunction with the high R_n value (MΩ) can lead to significant voltage drops (hundreds of mV) that may impact the current mirror ratio. The gate leakage increases steeply with the gate voltage level. In the selected 0.13 μm CMOS process the NFETs have $I_{g\_\text{leak}} = 0.1\,\text{nA}/\mu\text{m}^2$ at $V_{\text{gate}} = 1.5\,\text{V}$, $I_{g\_\text{leak}} = 25\,\text{pA}/\mu\text{m}^2$ at $V_{\text{gate}} = 1\,\text{V}$, and $I_{g\_\text{leak}} = 5\,\text{pA}/\mu\text{m}^2$ at $V_{\text{gate}} = 0.5\,\text{V}$ at the room temperature. This issue is even more problematic in further scaled CMOS technologies (e.g., 90 nm and 65 nm CMOS). The leakage currents of the NFETs and the PFETs do not track over process and temperature. PFETs tend to have lower leakage currents, which may lead to a large mismatch between the pump-up and pump-down current. The PLL loop responds in lock conditions by introducing a static offset between the reference and the feedback

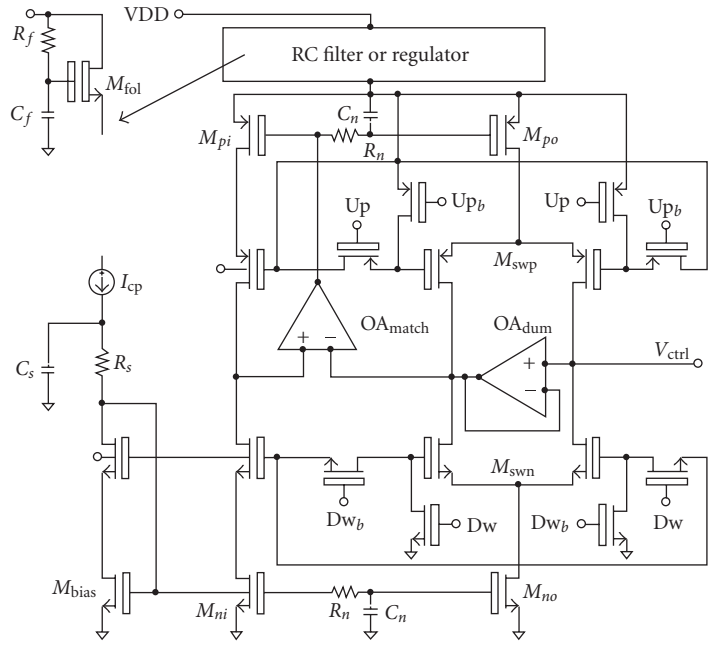

Figure 9: Dynamic current-matching charge-pump with supply and bias noise filters.

clocks. The equilibrium point is reached when the charge injected by a wider pulse, low value pump current is balanced with the charge injected by the narrow pulse, higher value complementary pump current. The large duty cycle of one of the charge-pump currents determines a significant degradation of the CP noise contribution, and if the wider pump current is the PFET one, then it also increases the supply noise and spur injection. To avoid gate leakage induced current mismatches, the M_{ni}/M_{no} and M_{pi}/M_{po} are implemented also as thick gate oxide devices, which have a negligible gate leakage current. Large-area devices were used to reduce their $1/f$ noise component.

A unity gain buffer OA_{dum} is usually used to keep the dummy side of the current steering charge-pump at the same potential with the active output (loop filter side). This minimizes the charge-sharing from the dummy side and thus reduces the ripple on the loop filter due to sharing current glitches when the output switches are ON. The noise of this buffer is first sampled on the parasitic capacitances from the common source points of the differential current steering switches when the dummy switches are ON, and is then shared with the loop filter when the output switches are ON. To minimize the OA_{dum} noise contributions a very large ratio needs to be maintained between the loop filter capacitance and the parasitic capacitance at the common source node.

Reducing the pump-up/pump-down current mismatches is key for a low reference spur level. A dynamic current matching feedback loop was implemented by adding the OA_{match} amplifier to drive the gates of the PFET current mirrors such that the NFET and PFET currents are well balanced [19, 28]. The ripple from the dummy side of the charge-pump (followed by the OA_{dum} wide-bandwidth operational amplifier) does not modulate the charge-pump PFET current since both the R_n, C_n filter and the low OA_{match} bandwidth are strongly attenuating it. The dynamic charge-pump current matching circuit consists of two feedback loops: a negative feedback given by OA_{match} and M_{pi} and a positive feedback given by $OA_{match,}$ M_{po}, and M_{swp} with OA_{dum} buffer. The low impedance provided by OA_{dum} buffer at the inverting input of the OA_{match} operational amplifier guarantees that the negative feedback has a much stronger loop gain in comparison with the positive one.

Maximizing the voltage swing at the charge-pump output requires the reduction of the number of stacked devices in the NFET and PFET current mirror legs. Cascode tail current mirrors are preferred for their much larger output impedance and thus a lower up/down current mismatch due to the variation of the loop filter voltage. However, cascode current mirrors take a larger voltage headroom that adds to the voltage drop on the ON-state switch to give the minimal output voltage level. Present design proposes a much higher output voltage swing charge-pump in which the M_{swn} and M_{swp} switches are operated between OFF and saturated ON states, such that they act as cascode devices when they are ON. The current steering operation is determined by the state of the two switches connected to the gates of the differential pair, providing either the cascode bias to the gates of M_{swn}/M_{swp} devices, or connecting them to ground. Eliminating one device from the stacked telescopic architecture of the charge-pump is particularly advantageous for the high charge-pump currents applications.

The noise coming from the supply lines is also sampled by the low duty-cycle switching waveform, determining a reduction of its power. Similar to the charge-pump devices internal noise, the supply injected white noise suffers aliasing, while the supply $1/f$ noise does not. If a supply filter or a

regulator is used to bias the charge-pump, its $1/f$ and white noise need to be carefully looked at.

A second concern for a charge-pump is its spur down-conversion capability. The switching action of the charge-pump switches has a chopping operation that results in a frequency translation (mixing). Therefore the high-frequency spurious tones present on the charge-pump supply voltage or bias current are downconverted around the f_{ref} PLL reference frequency. The resulting low-frequency ripple of the VCO control voltage determines spurs around the multi-GHz output clock. If these spurious tones fall inside the PLL bandwidth, where no rejection is presented by the feedback loop, they are simply amplified by the large N feedback divider modulus. In PLLs having low XTAL frequencies and high output clock frequencies (large frequency multiplication factor), these spurs may be the dominant spur mechanism.

The charge-pump presents this mixing property both to the supply voltage and the input bias current high-frequency spurious tones. The R_n, C_n CP noise filters also help rejecting the high-frequency spurs coming from the bias current. If additional rejection is required, a supplementary filter R_s, C_s can be added in series with the input bias current (I_{bias}). To minimize the supply ripple, an RC filter or a regulator can be used to bias the charge-pump. Reducing the VCO gain requires the maximization of the voltage swing at the CP output (1.3 V for thin gate oxide FETs). Using a regulator to bias the CP takes at least 0.5 V of headroom, which may be too much, particularly in the low-voltage applications. This design uses an active RC filter built with a zero-V_T NFET, which takes only 200 mV of voltage headroom and provides in excess of 40 dB of rejection for the high-frequency supply spurious tones. In this application the 1.8 V digital supply is sufficiently high to accommodate a 0.2 V voltage drop on the active filter and the 0.3 V headroom required by the PFET cascoded charge-pump current source.

10. LOOP FILTER

The main functions of the loop filter are to provide the PLL stabilizing zero and to filter the ripple on the VCO control voltage. Passive RC filters are widely used [2, 5, 6] due to their simplicity and their excellent power supply noise rejection. A passive loop filter has no supply lines, the only supply injected noise is coming from the charge-pump supply line. This is minimized by ensuring a CP output impedance much larger than the loop filter impedance at the spur frequency. The major drawback of the passive filters is their large capacitor size, particularly in low PLL bandwidth applications. These capacitors are often implemented off-chip, increasing the external component count and exposing the sensitive VCO control line to parasitic magnetic coupling due to the connection bondwire and package lead [5, 6]. Active loop filters were used to reduce the size of the loop filter capacitor [19, 21, 22]. A further reduction was brought by implementing a Miller capacitance multiplication technique [1]. This magnifies the size of the physical loop filter capacitance, allowing the on-chip realization of a large PLL time constant. However, the Miller capacitance gain comes also with a magnified noise from the Miller amplifier, this solution being suited only to mid noise performance PLLs. Furthermore, an active loop filter requires a supply line, resulting in a noise coupling path from the supply to the sensitive loop filter output node. To minimize the supply noise injection, the active loop filters are often biased from a dedicated high PSRR regulator [3, 4]. Reducing the gain of the oscillator and thus reducing the noise contribution of the PLL front end requires a very wide range voltage swing at the VCO control line. This in turn results in a large supply voltage requirement that prevents the usage of the dual-regulator technique. A single regulator needs to be used to bias the loop filter. A PFET output series regulator has the advantage of a low-voltage drop, but achieves a rather poor PSRR performance at medium and high frequencies. In contrast, an NFET output series regulator provides a higher PSRR up to high frequencies, but requires a larger voltage drop (at least a $V_{\text{GS}} + V_{\text{on}} = 0.7$ to 1 V). In modern deep-submicron CMOS processes the native NFET devices that do not undergo the threshold adjustment implantation have threshold voltages close to 0 V. Using them to build series NFET regulators results in a low-voltage drop and a high PSRR up to few tens of MHz [11]. Figure 10(a) shows one solution for realizing a very high PSRR series regulator for biasing an active PLL loop filter. The total voltage drop on the regulator is about $2V_{\text{on}}$ ranging from 0.3 to 0.5 V, depending on the supplied current. To further improve the PSRR of the regulator at high frequencies, a supplementary active RC filter R_f, C_f, M_{fol} was used to filter the noise from the drain of the main series regulator output device M_{nreg}. An effective supply noise filtering requires that the corner frequency of the active RC filter be with at least one decade below the PLL natural frequency. In wideband PLLs (BW $>$ 1 MHz) this can be easily achieved with an on-chip C_f capacitor. In low PLL bandwidth applications (BW $<$ 100 KHz) the active RC filter presented in Figure 2(c) needs to be used, since it has a decent PSRR staring from DC.

Figure 10(b) presents an alternative solution for integrating the loop filter on-chip. The proposed loop filter uses a passive feedforward RC filter that consists of two charge-pumps: the integral one CP_{int} that injects its current in the integral capacitance C_i and a proportional one CP_{prop} that injects its current into the R_z series resistance [12]. Active loop filters use a summing amplifier to add the integral and proportional control path signals [20]. This degrades the PLL phase noise due to the amplifier internal noise and also exposes the VCO control line to further supply noise injection. Alternatively in the case of LC-VCOs a split varactor can be built that performs the summation of the two control paths signals [23]. In the proposed passive feedforward loop filter the summation is realized by simply placing the C_i capacitance in series with the R_z resistor. To allow the flow of the proportional current through the R_z resistor, it needs to be connected towards the ground, while the C_i capacitor is connected floating (opposite to what is done in a standard passive RC filter). A ripple filtering capacitance C_p was added to reject the ripple from the VCO control line. A second-high frequency pole is realized with the R_{p2}, C_{p2} filter that further

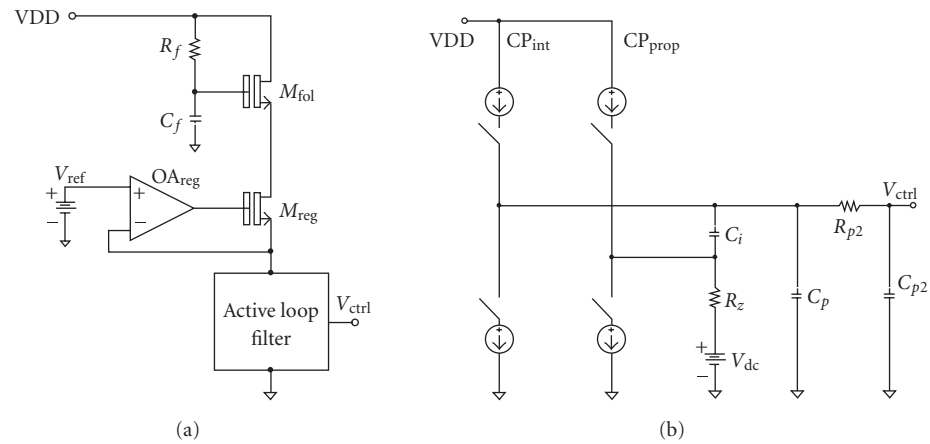

Figure 10: PLL loop filters: (a) active filter with high PSRR regulator; (b) passive feedforward filter.

rejects the high-frequency noise and spurious tones. The stabilizing zero position is given by

$$f_z = \frac{1}{[2\pi \cdot C_i \cdot R_z \cdot (1 + I_{\text{cpp}}/I_{\text{cpi}})]}, \tag{1}$$

$$R_{z\_\text{eq}} = R_z \cdot \left(1 + \frac{I_{\text{cpp}}}{I_{\text{cpi}}}\right). \tag{2}$$

The equivalent R_{z_eq} resistance appears multiplied by one plus the ratio of the two charge-pump currents, factor that can be designed to be as high as 20 to 30. However, the noise of the R_z resistor is not multiplied in this passive feedforward architecture, which brought the name of noiseless resistor multiplication loop filter. As the resistor is multiplied by a large factor, for a given PLL bandwidth the required loop filter capacitance is reduced by the same amount, allowing its easy on-chip integration.

If the R_z resistor is connected directly to ground, the potential at the output of the proportional charge-pump at the beginning of its ON state is 0 V, resulting in a triode-mode operation of the charge-pump NFET current mirror. This brings a large up/down current mismatch in the proportional charge-pump that is compensated by the PLL loop by locking with a large static phase error. In such conditions a large ripple appears at the VCO control line, degrading significantly the PLL reference spur performance. To avoid this spur degradation mechanism, the R_z resistor was connected at a low noise V_{dc} voltage generator that guarantees the saturation operation of the NFET current mirror during the entire charge-pump current pulse. This results in a good up/down current matching and thus a very low loop filter voltage ripple. The V_{dc} source can be implemented with several diode connected devices biased by a V_T/R current coming from a well filtered and/or regulated supply voltage, such that the supply noise injection is minimized.

Ensuring a low PLL phase noise profile at low offset frequencies (where the charge-pump current noise contribution dominates) requires a large $I_{\text{cp\_int}}$ integral charge-pump current (hundreds of μA). This increases the required size of the loop filter capacitance, growing its die area. Also the R_z resistor multiplication factor is limited by the headroom constraints on the proportional charge-pump that operates at a very large current level (several mA), and therefore has larger device V_{on} values.

The single slight drawback of the proposed passive feedforward loop filter is that it requires a floating C_i capacitance that needs to be implemented either as a MIM or as a metal interconnect capacitance. The large gate leakage of the deep-submicron FETs prevents their usage in PLL loop filters. The thick gate oxide FETs have a negligible gate leakage current and a higher capacitance density in comparison with MIM and metal capacitors, but they still cannot be used for the floating C_i capacitance due to their large bottom plate parasitic capacitance to the global IC substrate, which can bring a large substrate noise injection into the sensitive PLL loop filter.

The PLL loop filter can be realized with either a single-ended or differential architecture. A single-ended implementation benefits from a much lower die area (half the capacitor size in comparison with a differential architecture), but may suffer of substrate and supply noise injection. Differential implementations offer a better substrate and supply noise rejection, at the price of a twice as large loop filter area. Fully differential loop filters require both a differential charge-pump and a differential VCO tuning circuit, resulting in a more complex common-mode feedback circuit. Pseudodifferential architectures use two single-ended output charge-pumps controlled in opposite phase, such that when one is pumping up, the other one is pumping down [3, 4]. The loop filter capacitance is still twice as large, and an active differential-to-single-ended converter circuit is needed, but the oscillator has a simple single-ended tuning circuit.

Differential loop filters are mandatory in SOCs implemented in standard CMOS processes, where there are no other means of attenuating the substrate noise coupling from the noisy digital core. Modern deep-submicron CMOS processes offer a deep N-well option [30, 31] that can be used to build P-wells for the sensitive analog blocks that are isolated from the noisy global SOC substrate. This technique

can provide up to 40 dB attenuation to the substrate noise at GHz frequencies (depending on the deep N-well area). In this case the loop filter can be realized single-ended (large-area saving), since the substrate noise coupling is no longer an issue. To minimize the area of the deep N-well and thus reduce the parasitic capacitance to the global substrate, the loop filter resistors and the PFET switches are placed in a separate N-well, while only the loop filter capacitors and the NFET switches are placed inside the isolated P-well.

If an active loop filter is used, than the supply noise injection may be a concern. In this situation either a high value PSRR regulator needs to be used to bias the loop filter, or a differential loop filter can be implemented, since it has an intrinsic supply and ground noise rejection capability. The area of a regulator is usually much lower than the one of the loop filter capacitance. Therefore the regulator technique is preferred in moderate supply voltage applications (e.g., > 1.8 V). In low-voltage applications (1 V and below) there is no available voltage headroom to insert a regulator, making the differential loop filter a mandatory choice.

Ground noise can be also a major source of PLL phase noise degradation. If the VCO and the driving loop filter that generates its control voltage (V_{ctrl}) are separated by a large distance, such that their local grounds may have different dynamic potentials (e.g., due to currents that are injected in the ground line), then this noise voltage appears in series with the oscillator control voltage and is upconverted in spurs and phase noise skirts around the carrier. Present design uses dedicated supply and ground connections for the PLL oscillator, while a star-connected ground layout with no injected currents was used for the VCO and loop filter, guaranteeing that their local grounds are at the same dynamic potential all the time. The passive loop filter architecture ensures a very high supply noise rejection, while the deep N-well isolation allows a single-ended implementation, bringing a large-area saving.

11. LOW PHASE NOISE LC VCO

The top-level diagram of the proposed low phase noise multi-GHz LC-VCO for dual-band 802.11 a/b/g SOCs is presented in Figure 11. Using a single 5 GHz oscillator for both communication bands and deriving the 2.5 GHz clock via a divide by two of the main system clock results in a larger VCO tuning range and therefore a degraded PLL phase noise and spur performance. Present design uses two separate LC-VCOs having the tuning ranges of 2.4-2.5 GHz and 5.15–5.85 GHz, respectively. The larger area required by the two caged inductors was compromised to minimize the VCO tuning gain. An on-chip planar inductor built with a top-level thick metal layer was used for the LC oscillator tank. To minimize the parasitic magnetic coupling to the VCO coming from the large number of SOC's digital biasing and high-speed signal bondwires, the inductor was placed inside a metal cage using the top most thick metal layer. The proximity between the inductor and the metal cage reduces somewhat its quality factor (around 10), degrading the VCO phase noise. However, the good isolation from the large amount of

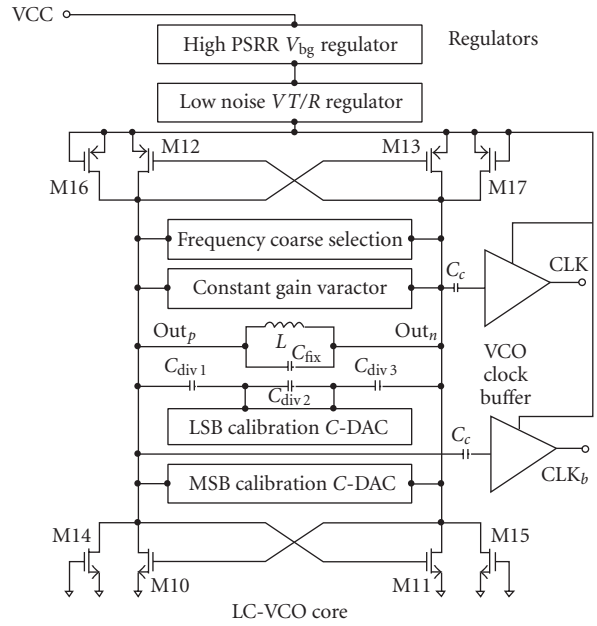

Figure 11: VCO top-level diagram including frequency calibration and tuning.

parasitic magnetic fields existent in a mixed signal SOC is far more important for a VCO operating in such a noisy environment than the slight degradation of the oscillator phase noise. To ease the frequency calibration process and also minimize the oscillator phase noise, the inductor value needs to be minimized, while the tank capacitance value needs to be maximized. Most existing oscillators use differential amplifiers with a tail current source [24–26]. Their drawbacks are first a reduced oscillating amplitude, which penalizes the signal to noise ratio, and second the tail current $1/f$ and thermal noise up- and downconversion, resulted from the VCO amplifier switching action. Both effects penalize the VCO phase noise performance. Noise filtering was used at lower frequencies [24] to reduce the tail current noise impact. However, this method is not viable for high multi-GHz oscillators (5–10 GHz) due to the lack of high value inductors having high self-resonating frequencies (>10–20 GHz). The oscillator core was realized with a CMOS amplifier having both NFET (M10,11) and PFET (M12,13) cross-coupled differential stages. A grounded source stacked NFET and PFET amplifier was used to minimize the VCO power consumption resulted due to the larger transconductance achieved for a given current budget [19, 23].

The amplitude of oscillation depends on regulator's output voltage V_{reg}, tank's losses R_L, amplifier's equivalent threshold voltage V_{theq}, and transconductance g_{meq} [15, 29]:

$$A \cong \frac{3}{8}\left(1 - \frac{1}{g_{m_{\text{eq}}} \cdot R_L}\right) \cdot V_{\text{reg}} + \frac{3}{8} \cdot \frac{1}{g_{m_{\text{eq}}} \cdot R_L} \cdot V_{\text{theq}}. \quad (3)$$

Therefore by adjusting the V_{reg} voltage the amplitude of oscillation can be altered. The oscillator uses a typical initial positive feedback loop gain of 2 (1.5–3 over process and

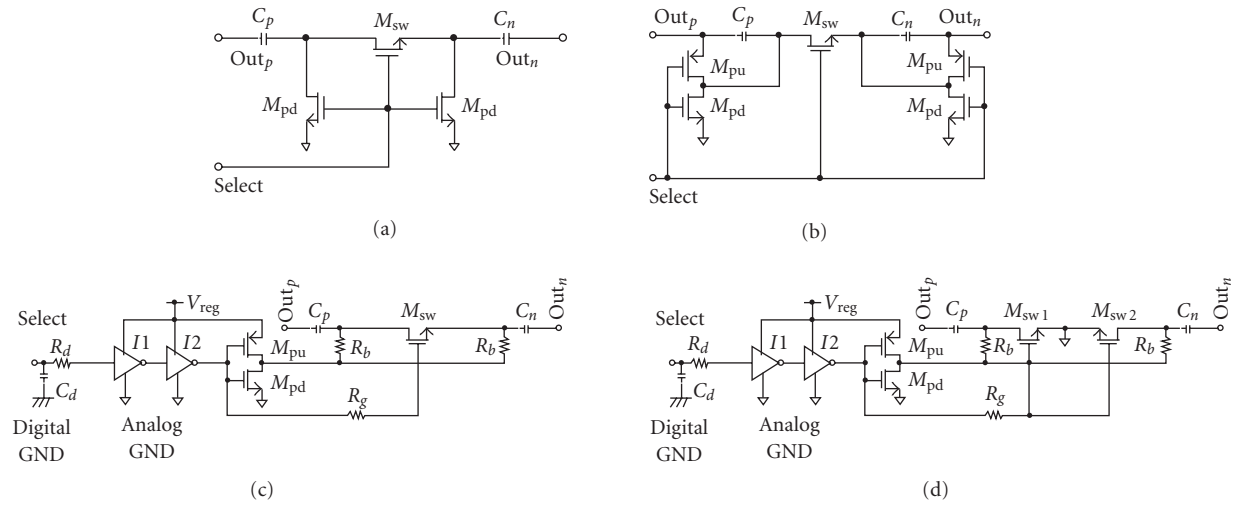

Figure 12: Frequency calibration capacitor legs: (a) all-NMOS switch, (b) CMOS switch, (c) CMOS switch with reduced pushing, and (d) CMOS switch with higher breakdown.

temperature corners) which ensures both a safe start-up and also achieves a minimum in the phase noise characteristic. Optimizing the VCO phase noise performance requires the maximum VCO amplitude within a given supply voltage budget and the process limited device breakdown voltage. The oscillating amplitude has a relatively low process and temperature variation, avoiding the need for an automatic amplitude control loop.

To minimize the supply injected spurs, a high PSRR regulator is required to isolate the LC-VCO from the global supply lines [15]. The regulator needs to have a very low output noise voltage in order to limit the oscillator phase noise degradation via the supply pushing mechanism. The nonlinear voltage-dependent capacitances from the amplifier output nodes set the supply pushing level higher than few MHz/V, value that dominates the oscillator phase noise performance. Achieving phase noise levels as low as −120 dBc/Hz at 1 MHz offset requires supply pushing levels lower than 100 KHz/V. The amplifier gate capacitances have a positive voltage coefficient, while the drain-to-bulk capacitances have a negative voltage coefficient. A supply pushing cancellation architecture was implemented with gate to source shorted NFET and PFET dummy devices connected at the two output nodes of the oscillator (M14–17) that have a negative voltage coefficient, which together with the drain diffusion capacitance of the main amplifier and the frequency calibration network, cancel out the gate capacitance positive voltage coefficient. A perfect compensation is possible only for a given design corner. Over the PVT corners a residual voltage coefficient will result. The key to a low supply pushing gain is to maintain this residual voltage coefficient under a certain safety limit.

The clock edges need to be fast enough when transitioning between two power supply domains (e.g., the transition from the VCO analog ground to the digital divider ground). To ensure enough gain for the multi-GHz clock, a clock buffer biased from the same clean VCO supply was used. The buffer supply current spikes are perfectly synchronous with the VCO output clock and therefore the buffer can share the same supply with the VCO without degrading its phase noise.

11.1. VCO frequency calibration network

Reducing the frequency synthesizer output clock phase noise requires a minimization of the oscillator gain. The targeted $0.25^{\circ}_{\text{rms}}$ double-sided integrated phase noise (between 1 KHz and 10 MHz) requires an oscillator gain around few tens of MHz/V, which with a 1.3 V tuning voltage range (limited by the MOSFETs breakdown voltage) results in a relatively low-frequency tuning range. To achieve a functional oscillator over all process, temperature, and supply voltage corners, while using a narrow tuning range varactor, requires a high-resolution frequency calibration network. The temperature variation of the oscillating frequency is about 0.2%, while a low supply pushing gain was achieved by using a pushing cancellation circuit. Reducing the VCO tuning range requires a low-frequency error, imposing a 0.1% frequency calibration resolution, which turns into a 0.2% frequency step. At the maximum operating frequency the 0.2% frequency step requires a 5 fF unit capacitor in the frequency calibration network for the selected inductor value.

There exist several solutions to realize the switches for the frequency calibration network. Figure 12 presents the most popular existing switch implementations, together with the solution used in the present design. The all-NFET switches architecture presented in Figure 12(a) is widely used in integrated VCOs [25, 26]. It consists of a main NMOS differential switch (M_{sw}) that provides a low on-state resistance to connect the two capacitors C_p and C_n to the LC tank, and two pull-down large L/W aspect ratio NFET devices (M_{pd}) that bring the drain and source of the main switch to ground when it is ON. This maximizes M_{sw} switch overdrive voltage, leading to a minimum R_{on} resistance for a given supply voltage headroom. The high on-state resistance of the M_{pd}

devices is not an issue since they provide only a DC level. The drain diffusion capacitance of the M_{pd} devices adds to the diffusion capacitance of the main switch (M_{sw}) to give the total nonlinear capacitance presented by the calibration leg to the LC tank. When the main switch is OFF, its drain and source are floating, their potential being set by the leakage currents. Having floating nodes in the calibration leg is not acceptable. If these potentials are driven to ground (e.g., by the NFET switches drain and source diffusion diodes leakage current), then at the maximum negative amplitude of the oscillation there is a risk of turning the drain and source diodes of the switches ON. This may lead to a significant loading of the LC tank and thus a severe degradation of the VCO phase noise.

Figure 12(b) shows one possible solution to resolve the floating nodes potential. It uses two pull-up PFETs (M_{pu}) in parallel with the C_p and C_n capacitors of the calibration leg [23]. When the leg is not selected, these PFET switches short the floating nodes to the collectors of the VCO amplifier, providing a known potential level. Long and narrow channel PFETs were used to reduce the nonlinear capacitance shown to the LC tank, since their large R_{on} resistance is of no concern. When the main switch (M_{sw}) is OFF, it is required to present a minimum parasitic capacitance to the LC tank. The M_{pu} PFETs pull the source and drains of the M_{sw} switch to the positive supply ensuring a minimal diffusion capacitance. The NFET pull-down and PFET pull-up devices constitute an inverter that drives the drain and source nodes of the main switch. The drawback of this implementation is the larger nonlinear capacitance shown to the LC tank due to the usage of two inverters per capacitor leg.

Figure 12(c) presents one solution to reduce the nonlinear capacitance shown to the LC tank by replacing the two pull-up/pull-down CMOS inverters connected in the signal path, with a single inverter connected at the common-mode voltage [15]. The parasitic capacitances of the pull-up and pull-down devices are further isolated from the main switch with the high value R_b bias resistors. A moderately large value R_g resistor was connected in series with the gates of the MOS switches in order to isolate the drain diffusion output capacitance of the driving inverter from the frequency calibration leg. In a perfectly symmetric circuit this would have no impact since it is connected to an AC ground node. In reality any imbalance in the frequency calibration leg will reflect a fraction of the gate inverter nonlinear output capacitance (need to be kept negligible) back on the LC tank.

The digital gate control signals that determine the ON or OFF state of the MOS switches in the calibration network come from the digital core of the IC and are referenced to the digital supplies, which carry a significant amount of noise. To avoid the noise leakage from the digital ground into the analog ground of the VCO, each digital control line has a dedicated R_d, C_d filter. The series resistance R_d increases the impedance looking towards the analog circuit, preventing the digital noisy current from going into the analog VCO ground, while the C_d capacitor connected at the digital ground closes locally the digital noise. To avoid noise coupling from the positive supply of the digital circuit, each digital control line is buffered with two inverters biased from the same low noise and high PSRR regulator used by the LC-VCO core. If the buffers would have been biased from the noisy global PLL supply, then the variation of the V_{CC} supply voltage would propagate to the gates of the MOS switches, causing a parasitic modulation of their series channel resistance. Considering the parasitic capacitance of the MOS switch and the MIM capacitor of the calibration leg, the LC tank sees an RC network having three series connected capacitors from which the centre one that has a much smaller value is shorted by a voltage controlled resistor (M_{sw} switch). Such a network is equivalent to a voltage controlled capacitor that appears in parallel with the LC tank and determines a parasitic modulation of the oscillating frequency. This variable capacitance results in an upconversion of the supply noise and spurs around the VCO carrier, degrading its phase noise performance. To solve this issue, a regulated voltage (V_{reg}) was used to bias the inverters that buffer the digital control lines going to the MOS switches of the calibration network. Since there is no dynamic current going through these static input inverters of the frequency calibration network, they can be connected to the same regulator used by the LC-VCO core.

Using a differential switch has the advantage of providing the minimum series resistance for a given supply voltage level and a targeted MOS switch parasitic capacitance value. However, the switch is exposed to the large peak-to-peak differential swing of the oscillator. Optimizing the VCO phase noise requires the maximization of this voltage. The targeted -100 dBc/Hz phase noise at 100 KHz offset requires a 3 V differential peak-to-peak amplitude that cannot be sustained by a single MOS switch in the calibration legs. A low phase noise oscillator design should have the single-ended amplitude as close as possible to the available headroom voltage. An optimal architecture should provide equal voltage stresses for all MOS devices from the VCO amplifier and from the frequency calibration network and tuning varactor. For the calibration leg shown in Figure 12(c) the MOSFET switches are the amplitude limiting factor [15]. Figure 12(d) presents a higher amplitude version of the single CMOS inverter-driven differential switch. It uses two grounded source switches (M_{sw1} and M_{sw2}) instead of a single differential switch (M_{sw}). This doubles the maximum differential voltage sustained by the calibration leg allowing the required 3 V peak-to-peak differential swing. The price paid is doubling the series resistance and thus halving the quality factor of the calibration network. As there is no DC current in these MOS switches, they can tolerate a larger drain-to-source voltage (e.g., 1.5 V) than the process recommended maximum voltage (1.3 V).

The frequency calibration range needs to cover the 10% process variation coming from both inductor value inaccuracy (small) and the tank capacitance variation (usually the dominant factor). Achieving a wide calibration range, while achieving the 5 fF capacitor step, requires at least an 8-bit resolution in the frequency calibration network. This is generally implemented as a capacitor DAC that switches the appropriately sized capacitor legs in or out of the LC tank. To accommodate the 40 fF minimum size MIM capacitor, while achieving a 5 fF unit capacitor step, a differential capacitor structure (doubles the minimum required capacitance

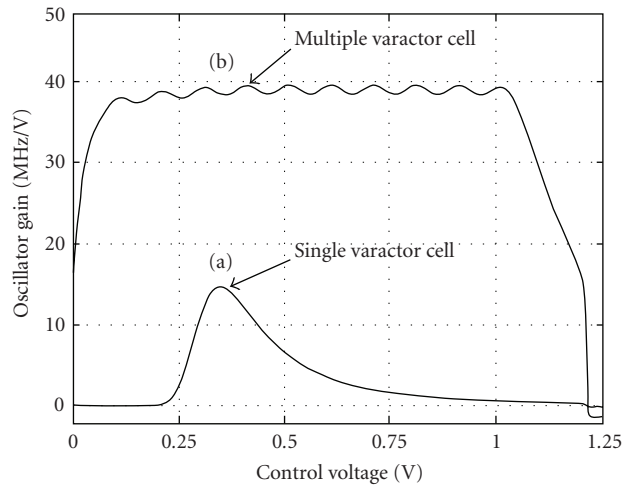

Figure 13: (a) Single accumulation-MOS varactor tuning gain; (b) multiple parallel-connected varactor cell with quasiconstant tuning gain.

unit) was used in conjunction with a 2-to-1 capacitor tap (see Figure 11). A 2-to-1 tap reduces the size of a capacitor connected to it by a factor of four when reflected back on the LC tank. The 8-bit frequency calibration DAC was split in two sub-DACs: an LSB-DAC connected at the 2-to-1 capacitor tap and an MSB-DAC connected directly on the LC tank. A minimum of two LSB bits need to be connected at the 2-to-1 tap in order to achieve the required 5 fF capacitor step. The accuracy of the MIM capacitors degrades sharply when going towards their minimum 40 fF size. Furthermore, maintaining a high-quality factor for the LC tank requires large-area series MOS switches that have sizable parasitic capacitances, which may limit the calibration resolution if they become comparable with the switched MIM capacitor size. To achieve a good monotonicity of the capacitor DAC, four LSBs where connected at the 2-to-1 tap, while the four MSBs were connected directly on the LC tank. Overlapping between the adjacent frequency ranges was built-in the capacitor DAC, such that the calibration algorithm can recover from decision errors. At each decision step of the successive approximation register (SAR) algorithm, the amount of capacitance that is left unswitched in the DAC is slightly higher than the capacitance that is switched in or out of the LC tank. Therefore if an erroneous decision of switching-out a capacitor is taken in a previous calibration step (e.g., due to a supply glitch), then there is enough capacitance left unswitched to achieve the desired value of the LC tank capacitance.

11.2. Constant gain Varactor

Figure 13(a) illustrates the tuning gain variation of a single accumulation MOS capacitor which has a bell-shape characteristic. A wide variation of the tuning gain requires a more sophisticated PLL loop filter in order to achieve a constant damping factor and loop bandwidth over the entire frequency range. To solve this issue, several MOS capacitors were connected in parallel, while their control voltages are shifted such that the individual peak tuning gain points are uniformly distributed over the entire control voltage range (Figure 13(b)). The equivalent tuning gain has an almost constant plateau, the gain ripple depending on the number of parallel cells. This design uses ten MOS capacitors in parallel to achieve less than 15% tuning gain ripple over all design corners.

Figure 14 presents the detailed schematic of the constant gain varactor. A differential varactor cell was built using two accumulation MOS capacitors $C_{\text{varpi}}/C_{\text{varni}}$, having the gates connected towards the LC tank and the wells going to the loop filter control voltage (V_{ctrl}). To prevent the discharge of the loop filter integration capacitance due to the significant leakage current of the MOS capacitors bulk, a simple source follower buffer stage was interposed between the loop filter and the varactor control node. The MOS capacitors are AC coupled to the LC tank using the $C_{\text{cip}}/C_{\text{cin}}$ fixed capacitors. This allows a separate DC bias voltage to be brought to the gate of each individual MOS capacitor, which shifts the position of the corresponding peak gain point. The R_p resistors keep floating from the signal perspective the nodes between the AC coupling capacitors and the MOS capacitor. The simplest way to generate the offset voltages is using a resistor divider biased from the low noise VCO regulator. The noise of the resistor divider may significantly impact the VCO output phasenoise. Filtering capacitors can be used to limit the divider noise contribution, their main drawback being a large required capacitor area. To reduce the supply spur injection through the resistor divider, present design has implemented a switched capacitor bias network. The voltage levels generated by the resistor divider ($R_{\text{div 1–10}}$) are sampled periodically on a set of storage capacitors ($C_{\text{div 1–10}}$) at a low-frequency rate. Transmission gate switches $T_{g1–10}$ were used to sample the offset voltages ($V_{\text{off1–10}}$) on the corresponding storage capacitors. The C_{divi} capacitors were connected directly to the gates of the accumulation MOS varactor. The main leakage components are given by the drain and source diffusions of the MOS varactors, which may results in a discharge of the C_{divi} storage capacitors. The ripple on the offset voltage

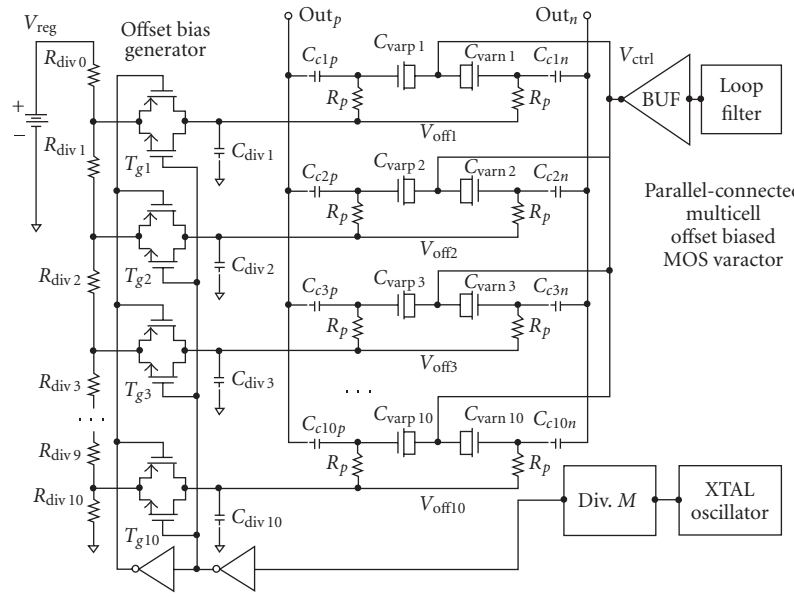

Figure 14: Quasiconstant tuning gain accumulation-MOS varactor using offset bias parallel-connected legs.

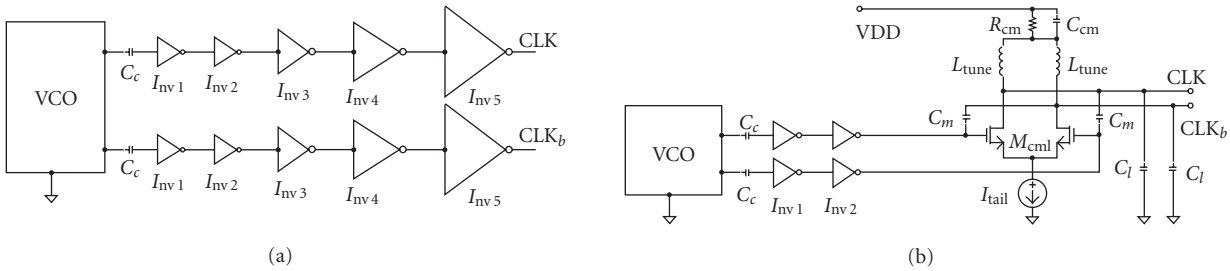

Figure 15: Output clock buffers using: (a) CMOS inverters; (b) tuned load CML inverter.

nodes leads to output spurs whose amplitude is proportional with the K_{vco} oscillator gain and inversely proportional to the refresh frequency $f_{refresh}$. The refresh rate of the switched-capacitor bias generator needs to be high enough such that the resulting voltage ripple is lower than $1\,\mu$V, which results in negligible spur (< -80 dBc). To minimize the ripple at the offset voltage nodes, each sampling switch has a pair of half-size dummy switches connected on its either sides to cancel (at least partially) the channel charge injection and reduce the clock feedthrough. The price paid is the twice as large leakage current due to the extra source and drain diffusions connected to the storage capacitors (C_{divi}). By having the sampling switches turnedoff most of the time minimizes the supply spur injection. The power of the injected tone is reduced by the sampling signal duty-cycle factor. To achieve a large attenuation, the sampling signal needs to have a very low duty cycle (1 to 5%).

12. VCO OUTPUT CLOCK BUFFER

The LC oscillator generates a low phase noise sine-wave with a 3 V peak-to-peak differential amplitude. The multi-GHz clock needs to drive both the frequency synthesizer divider and the RF front-end mixers. Furthermore, the kickback due to the digital circuits switching can be detrimental to the oscillator phase noise performance, mandating an isolation buffer between the VCO and its highly nonlinear load capacitance. This buffer has two main goals: first to square-up somewhat the VCO sine-wave and second to increase the drive capability of the clock path. At these high frequencies the achievable gain of a differential pair is fairly low (typically 3–10) even in high f_T deep-submicron CMOS processes. Therefore only a limited amount of clock waveform squaring is possible. Figure 15(a) shows a straight CMOS implementation of the VCO clock buffer that requires a large number of cascaded stages in order to achieve the desired capacitive drive strength. This solution takes a large supply current and is prone to clock pulse width distortion due to the device V_T mismatches. Figure 15(b) presents the detailed schematic of the proposed VCO output clock buffer.

The oscillator is biased from a dedicated supply to avoid supply noise injection. The driven mixers are operated from a separate supply. The finite mismatches between the devices in the clock path (transistors, resistors, and parasitic

capacitances) lead to a nonzero common-mode to differential gain. The transition between the two power supply domains needs to be performed inside the VCO clock buffer. If the transition is done at a point where the clock is still sinewave looking, the higher sensitivity to supply noise leads to a severe degradation of the clock phase noise.

To limit the crosstalk between the analog and digital supply domains, the first gain stages ($I_{\text{nv}1}, I_{\text{nv}2}$) of the clock buffer were built inside the VCO metal cage, while the third CML gain stage resides in the mixer core. The clock bus running from the analog to the digital section of the buffer is shielded with a coaxial metal structure connected to the analog ground. The length of the clock bus was minimized in order to reduce the parasitic capacitive loading at the clock lines. A high loading capacitance may result in a subsequent slowing down of the clock slew rate and expose again the signal to supply noise injection. The intrinsic noise of the different stages in the clock buffer path also contribute to phase noise. If enough gain ($A_v > 3$) is achieved in the first gain stage, then the phase noise degradation is dominated by the front-end stages. The edge squaring process is in fact a phase sampling action, which results in aliasing of the wideband noise from the front-end buffer stages. Once the clock edges are squared up, a proper sizing of the following stages with respect to their corresponding load capacitance needs to be used, such that they will not significantly slow down the signal transitions, which may create a second point of wideband noise aliasing.

Standard clock buffers require a large number of cascaded pseudodifferential inverter stages in order to drive large load capacitances (e.g., 1 pF). This leads to using a significant percentage of the IC power in the high-frequency clock path. Inductive peaking was used in the past to speedup the edges and thus reduce somewhat the power in the clock tree path. A larger power consumption reduction can be obtained by using an inductive tuned clock tree [27]. It consists of resonating the large load capacitance (C_L) with a shunt inductor (L_{tune}). Therefore the size of the last clock buffer stage can be much smaller, since it needs only to maintain the oscillating clock waveform. The load capacitance tuning was possible due to the narrowband nature of the clock. A reduced number of gain stages is required in a tuned clock path (only three in this application), further reducing the power consumption in the clock path. The inductive tuning of the clock tree trades delay for a higher edge slew rate. A special care needs to be devoted to the tuning inductor layout. The parasitic coupling between the clock buffer and the oscillator can significantly degrade the VCO phase noise, while the coupling from the oscillator to the clock buffer output stage may result in a large reduction of the clock amplitude due to the summation of two signals having the same frequency, but different phases. To reduce the parasitic magnetic coupling to the VCO-BUF tuning inductor, an inductor-in-cage structure was used, similar to the VCO tank inductor. The substrate coupling between the two inductors was reduced by placing a low doped native P-well layer below the inductors.

Fast clock edges require also a reduction of the capacitive load presented by the differential CML gain stages to the front-end driving inverters. Miller capacitance neutralization was used to achieve this goal [32]. It consists of connecting two capacitors (C_m) matched with the C_{gd} of the main gain stage devices from the gate of each differential pair device to the drain of the complementary device (cross-coupled capacitors). Therefore each input of the differential pair sees in essence two equal capacitors that have on the second terminal signals that are equal in value, but of opposite signs, resulting in a cancellation of the capacitor current from the input circuit perspective. The low value (few fF) Miller compensation capacitors were realized with metal interconnect capacitors (MIM capacitors have a minimum value of 40 fF in the selected CMOS process).

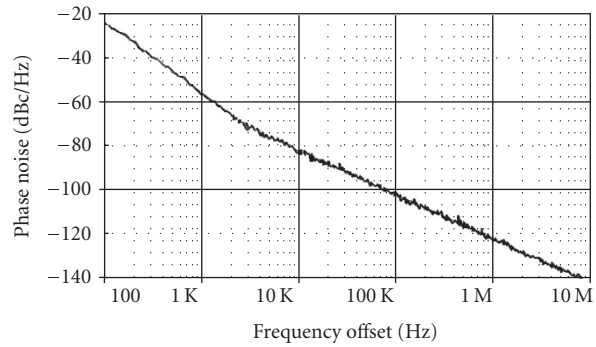

Figure 16: LC-VCO phase noise in open-loop operation.

13. EXPERIMENTAL RESULTS

The above-presented supply partition, filtering, and regulation techniques have been used to reduce the phase noise and coupled spurs of a 0.13 μm CMOS frequency synthesizer for a dual-band 802.11 a/b/g SOC. A low VCO phase noise degradation due to parasitic magnetic coupling and supply or substrate noise injection is crucial for meeting the transceiver sensitivity target. Figure 16 presents the open-loop phase noise plot of the 5 GHz oscillator, while the entire digital side of the SOC is active. The phase noise is lower than −120 dBc/Hz at 1 MHz offset from the carrier, when measured after the divide by two of the quadrature I/Q generator. This value is very close to the estimated VCO phase noise, based on the LC tank quality factor and oscillator amplifier noise figure, showing a negligible phase noise degradation due to supply pushing, substrate injection, and parasitic magnetic coupling. This proves that the dual-regulator architecture and the inductor-in-cage layout are effective in reducing the secondary phase noise degradation effects. A very low $1/f^3$ corner frequency was achieved (around 5 KHz), showing the effectiveness of the tail-free voltage-mode bias of the VCO, which eliminates the tail current noise upconversion.

Figure 17 presents the PLL output clock phase noise in the 802.11a mode, after a supplementary divide by 2 connected after the I/Q generator. A relatively large loop bandwidth (500 KHz) was selected in order to adequately reject any low offset frequency spur coupled to the VCO. This value is close to the optimum PLL bandwidth which is given by

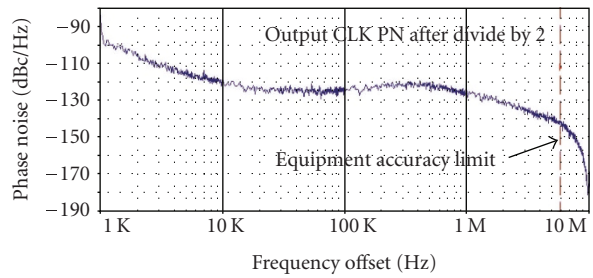

Figure 17: PLL output clock phase noise with entire digital core running.

the cross-over point of the VCO phase noise characteristic with the PLL front-end phase noise reflected at the PLL output. The in-band phase noise is −118 dBc/Hz, while the total phase noise integrated from 1 KHz to 10 MHz is as low as 0.25° rms, value that is substantially better than the 802.11 a/b/g requirement. The doted line in the phase noise plot represents the accuracy limit of the phase noise measurement equipment based on the delay line discriminator technique.

Figure 18(a) presents the close-in frequency spectrum and Figure 18(b) shows the far-out frequency spectrum of the PLL output clock after it is downconverted to a low IF frequency. The reference spurs are lower than −85 dBc, while the major spurs coupled from the digital blocks are lower than −78 dBc (ADC, digital PLL, and digital core). These low value coupled spurs prove the effectiveness of the multi-regulator PLL architecture. Figure 19 presents a detail of the 802.11 a/b/g SOC die photo, showing the frequency synthesizer floor-plan (the two caged inductors of the 2.5 GHz and 5 GHz LC-VCOs are not visible). A circular signal flow was used at the PLL top level, with minimal signal line lengths for the multi-GHz connections (VCO-to-BUF and BUF-to-Div.N) and with a longer length for the VCO control line that was shielded with a coaxial metal structure. One can observe that the different series and shunt regulators together with the test circuitry occupy about half the total PLL die area. However, this large area and the relative low-power efficiency are well justified by the excellent PLL noise and spur performance, while operating on the same die with a noisy digital core.

Modern CMOS processes offer a deep N-well option [30, 31] that can be used to isolate the local substrate of sensitive analog blocks from the noisy global SOC substrate. The key role of the deep N-well is to collect and direct towards the unregulated supply the noise injected capacitively by the noisy global substrate and prevent it from getting to the bulks of the NFETs, from where it may leak into the signal path through the device body effect. To achieve this goal, the series resistance of the N-well walls needs to be minimized. This can be achieved, for example, by breaking a larger deep N-well in several smaller deep N-wells that share the lateral N-well walls. Increasing the N-well walls perimeter reduces significantly the series resistance to the analog supply, making this the main closing path for the substrate injected noise. All major blocks inside the PLL are placed inside local P-wells connected to the clean analog ground, while the surrounding N-well ring and the deep N-well isolation layer are connected to the global (unregulated) supply and not at the regulator output in order to prevent the substrate noise contamination of the clean regulated voltages. To make effective the deep N-well isolation (at least 40 dB attenuation of the high-frequency substrate noise), its area needs to be kept to a minimum. Although placing the deep N-well layer under the N-well in which the PFETs are residing results in a more compact layout (shorter signal lines with lower parasitic capacitances), in mixed signal SOCs it is preferred to keep the PFETs outside the deep-N-well, in spite the large separation required between the NFETs deep N-well and the PFETs N-well. It is always preferred to close on-chip the magnetic loops (achieve a much lower loop area), rather than let the substrate noise to go off-chip through the V_{dd} supply bondwires and circulate in a large loop that is strongly dependent on the PCB layout. An even more dangerous situation is when the loop contains switching elements and the area of the loop changes in time at a given low-value frequency. This can result in large spurious tones in the LC-VCO due to the magnetic coupling between the tank inductor and the variable area parasitic loop. Using caged inductors help to some extent reducing this type of spurs. Bypass capacitors were used to close on-chip to ground the substrate injected noise. In mixed signal RF ICs that have digital cores operating at multi-GHz frequencies the deep N-well isolation is less effective, requiring a careful placement of the analog and digital blocks in the top-level layout floor-plan, a reduction of the deep N-well protected areas, and the use of low doped native layer moats to isolate the analog circuitry from the digital core. At very high frequencies (5–10 GHz) all the local substrates are shorted to the global substrate by the relatively large deep N-well parasitic capacitance. The smaller the area of a deep N-well, the larger the frequency up to which it provides a good isolation.

All major analog and digital blocks are surrounded by metal cages that attenuate the parasitic magnetic coupling. However, even the thick top metal layer of the selected 0.13 μm CMOS process offers only 15–20 dB attenuation to the magnetic coupling above 5 GHz. Both the VCO and VCO-BUF inductors are build inside metal cages in order to minimize the magnetic coupling from the surrounding bondwires, or any other magnetic loop present in the large SOC, reducing thus the spur and phase noise injection.

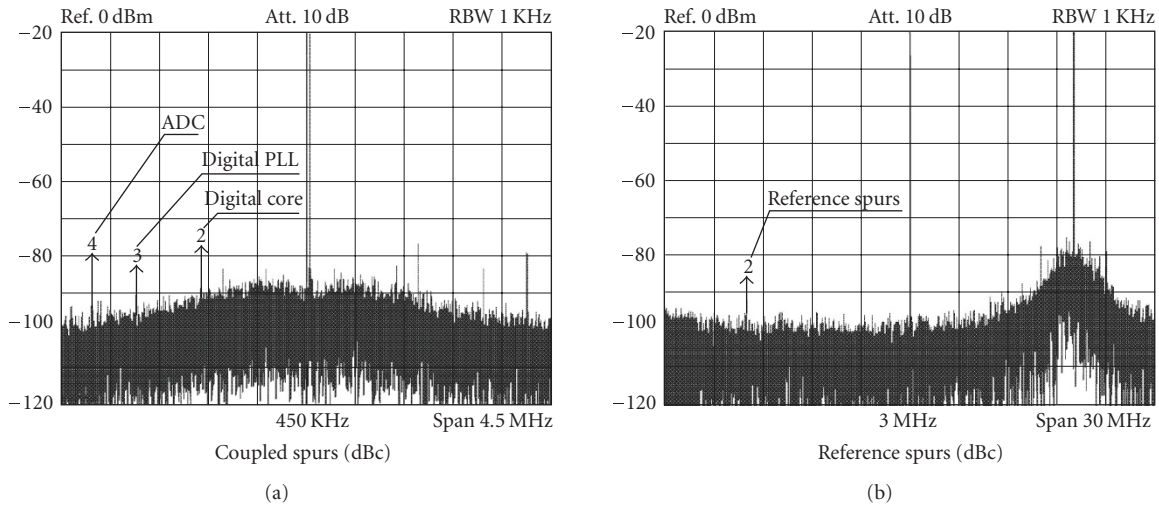

Figure 18: Output clock frequency spectrum: (a) close-in coupled spurs; (b) far-out reference spurs.

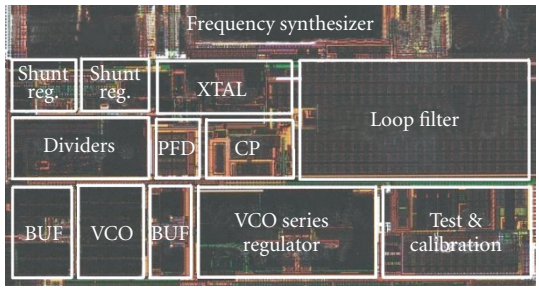

Figure 19: SOC die photo detail showing PLL layout floor-plan.

14. CONCLUSIONS

This paper presents several power supply partitioning, filtering, and regulation techniques aimed at supply noise and spur rejection in frequency synthesizers operating in large mixed analog-digital SOCs. To prove experimentally their effectiveness, they were implemented in a multi-GHz PLL operating in the same die with a dual-band 802.11 a/b/g SOC. The test chip was realized in a 0.13 μm CMOS process.

Keeping a clean global PLL supply and minimizing the noise and spur coupling between different analog and digital PLL building blocks requires that all supply current spikes generated by the digital circuits be closed locally with the help of dedicated shunt regulators having a high-value reverse PSRR. The boundary between the analog and digital supply domains was placed at the charge-pump high impedance output node, avoiding the leakage into the PLL signal path of the noise between the two supply domains. Series regulators were used to bias all sensitive analog blocks (XTAL oscillator and VCO) that require a supply line. To further improve the PSRR and noise performance of serial regulators, a dual-regulator architecture was proposed. A first wideband bandgap referenced regulator provides most of the PSRR performance, while a second narrow-bandwidth V_T/R referenced regulator was used to ensure a low output noise performance.

A passive feedforward loop filter was proposed that has an excellent PSRR rejection and also allows the on-chip integration of the loop filter capacitance. To minimize the PLL front-end noise and spurs sensitivity, the gain of the oscillator was reduced by using a high accuracy frequency calibration network that compensates for the process variation of the oscillating frequency. Furthermore, a virtually flat VCO tuning gain over the entire frequency range was ensured by using several accumulation MOS varactors connected in parallel and having the bias voltage shifted one from another, such that the individual $C(V)$ gain peaks are uniformly distributed over the entire VCO tuning range.

Using a dedicated series or shunt regulator for each PLL building block allows the SOC operation without the costly RC or LC off-chip filters on the frequency synthesizer supply lines, reducing significantly the external component count the proposed multiregulator PLL architecture delivers a very low 0.25°rms integrated noise, while the coupled spurs are lower than −78 dBc, performance that is compatible with the most stringent modern wireless communication standards.

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