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Transceiver Design for Multiband OFDM UWB

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Ultra-wideband (UWB) is an emerging broadband wireless technology enabling data rates up to 480 Mbps. This paper provides an overview of recent design approaches for several circuit functions that are required for the implementation of multiband OFDM UWB transceivers. A number of transceiver and synthesizer architectures that have been proposed in literature will be reviewed. Although the technology focus will be on CMOS, also some design techniques implemented in BiCMOS technologies will be presented.

1. INTRODUCTION

Short-range communication systems (so-called wireless personal area network (WPAN) systems) with ranges of up to 10 m are becoming popular in replacing cables and in enabling new consumer applications. Examples such as Bluetooth and ZigBee, which operate in the 2.4 GHz ISM band, have however a limited data rate, typically about 1 Mbps, which is insufficient for many applications like fast transfer of large files (e.g., wireless USB) and high-quality video streaming. In order to increase the data rate to several hundreds of Mbps, a higher bandwidth is preferred over a larger SNR. This became possible at the moment the FCC released spectrum for UWB in the US spanning from 3.1 to 10.6 GHz with an average transmit power level of only −41.3 dBm/MHz [1, 2]. Several proposals have since then been presented to realize a short-range high data rate communication link. At present, both direct-sequence impulse communication and multiband OFDM UWB systems are under consideration as a standard.

The standard proposed by the multiband OFDM alliance (MBOA) is based on subdivision of the large available bandwidth in subbands of 528 MHz (see Figure 1) [2]. The data is QPSK-OFDM modulated on 128 subcarriers. Various modes are defined with data rates up to 480 Mbps. In the mandatory mode of operation (Mode 1), a frequency-hopping scheme in the three lower bands is implemented. Using only the three lower bands allows the use of a bandpass prefilter to reduce the interferer level of the 5 GHz ISM band. After each symbol period of 312.5 ns, a 9.5 ns guard time is available for hopping to the next band.

This paper intends to give an overview of the current status in multiband OFDM-based UWB systems. Section 2 will discuss the most important system specifications. Section 3 will highlight the progress made on receiver building blocks and Section 4 will focus on transmitter building blocks. Various design aspects on the synthesizer will be discussed in Section 5. Several (fully) integrated transceivers will be discussed in Section 6 and finally some concluding remarks are stated in Section 7. Although the emphasis of this paper will be on progress that is made on implementations in CMOS technology, some BiCMOS transceivers and circuits will be discussed as well.

2. UWB TRANSCEIVER SPECIFICATIONS

UWB receiver design is challenging, as it simultaneously requires a low noise density in a large bandwidth and a high linearity since large interferers can be present close to the used frequency band. An interferer scenario is required to determine the amount of filtering needed. On the transmit side, the challenge is in achieving a tunable, flat gain response over a 1.584 GHz bandwidth. Probably the most challenging block is the synthesizer due to the fast-hopping requirement.

2.1. Receiver requirements

For the receiver, the noise figure (NF) can be obtained from the system NF_{system} according to $NF = NF_{system} - IL_{prefilter}$ with $IL_{prefilter}$ the insertion loss of the prefilter. For a three-band system, the MBOA proposal assumes an NF_{system} equal to 6 dB. For the 55 Mbps mode, this reflects a sensitivity level

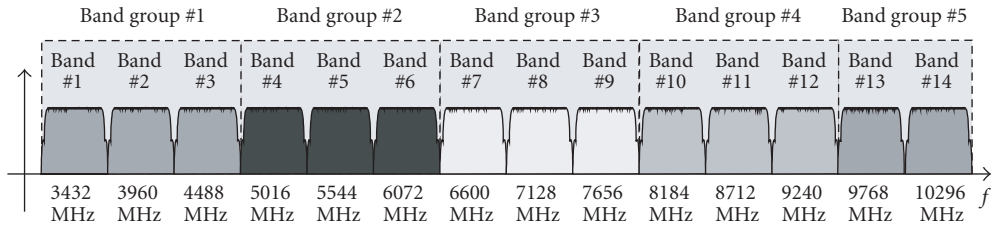
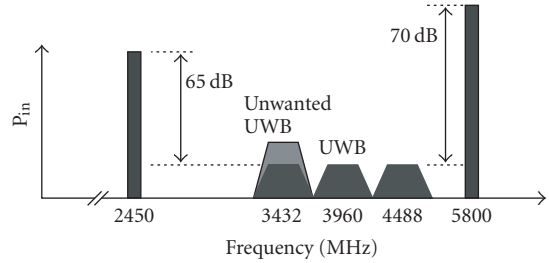


Figure 1: MBOA frequency bands and their partitioning.



Interferer scenario: (MBOA recommendation)

Distance wanted UWB:	10 m ⟶ −73 dBm
Distance WLAN interferer:	0.2 m ⟶ −3 dBm
Distance 2.4 GHz ISM interferer:	0.2 m ⟶ −8 dBm
Distance GSM1900 interferer:	1 m ⟶ −8 dBm
Distance unwanted UWB interferer:	2 m ⟶ −60 dBm

Figure 2: Interferer scenario. Indicated are received interferer powers.

of −83.5 dBm with an SNR of −5 dB. For the highest data rate of 480 Mbps, the SNR is 6 dB and therefore the sensitivity level is increased to −72 dB. To achieve graceful coexistence with other wireless technologies such as 802.11 WLAN and Bluetooth, an interferer robust receiver is needed. The MBOA interference scenario recommendation is depicted in Figure 2, indicating that even when a realistic 20 dB of prefiltering is taken into account, linearity requirements are severe. Most UWB systems target an input IP2 (iIP2) requirement above +20 dBm and an iIP3 requirement in the order of −9 dBm.

Due to the strong interferers, there are severe filter requirements at IF as well. Consider the case where the closest 802.11a interferer is located only 398 MHz away from the edge of subband #3 centered at 4.488 GHz (5.15 GHz − 4.752 GHz) at a distance of 0.2 m while the wanted UWB signal is transmitted from 10 m distance. In such a case the filter has to provide more than 35 dB of attenuation relative to DC at 662 MHz offset. In a similar way, for the upper band of 802.11a an attenuation of 46 dB is required at an offset of 1.3 GHz.

2.2. Transmitter requirements

A key requirement for a UWB transmitter is that the spectral density limit of −41.3 dBm/MHz must be met. Based on this emission mask and the frequency hopping specification, the maximum transmit power can be calculated as −9.5 dBm. Assuming a power loss of about 2.5 dB between antenna and PA, the power that needs to be generated is −7.0 dBm. Study on the effect of nonlinearity on OFDM signals indicates that a back-off of 2–4 dB ensures acceptable degradation [3].

2.3. Synthesizer requirements

As the radio has to cover at least the lower three bands as defined in the MBOA and since most likely a zero-IF architecture is used, the synthesizer needs to provide quadrature signals at the center frequencies of the bands at 3432 MHz, 3960 MHz, and 4488 MHz. The I/Q mismatch must be lower than −30 dBc. In the MBOA proposal, frequency hopping between two subbands occurs once every symbol period of 312.5 ns. This period contains a 60.6 ns suffix, which is followed by a 9.5 ns guard interval in which the frequency hopping should be accomplished. The demands on the purity of the generated carriers are also stringent due to the presence of strong interferer signals. All spurious tones in the 5 GHz range must be below −50 dBc to avoid down-conversion of strong out-of-band WLAN interferers into the wanted bands. For the same reason, the spurious tones in the 2 GHz range should be below −45 dBc to allow co-existence with the systems operating in the 2.4 GHz ISM band, such as 802.11 b/g and Bluetooth. Finally, to ensure that the system SNR will not degrade by more than 0.1 dB due to intercarrier modulation, the overall integrated phase noise should not exceed 3.5 degrees rms. This can be recalculated to a phase noise requirement of −100 dBc/Hz at 1 MHz offset from the carrier.

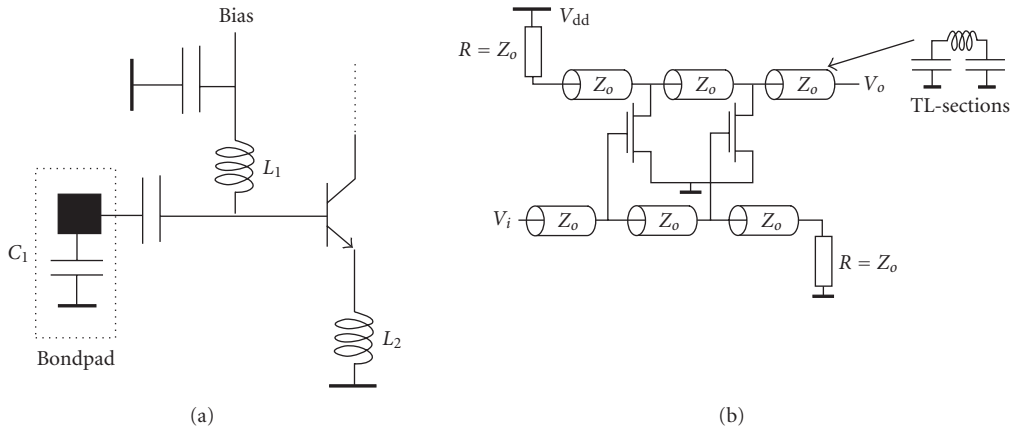


Figure 3: Several LNA topologies: wideband impedance matching (a); distributed LNA (b).

3. RF RECEIVER BUILDING BLOCKS

In addition to the receiver requirements, the low-noise amplifier (LNA) must provide broadband input matching and a broadband transfer. Several design options have been proposed in literature.

One possibility is to use a bandpass filter at the input in combination with an inductively degenerated (cascode) stage. In this way the reactive part of the input impedance will be cancelled over a wide frequency band [4, 5]. In Figure 3(a), L_1 together with C_1 form the shunt branch of the filter, the series branch is formed by L_2 together with the base-emitter capacitance [4]. Implemented in a 0.18 μm SiGe BiCMOS process, the LNA achieves an NF below 3 dB and an insertion gain above 20 dB.

Distributed amplifiers also achieve wideband behavior. Where in mm-wave design coplanar wave guides or striplines are used to implement the transmission lines, silicon implementations use integrated inductors and capacitors as the lumped element replacement circuits for the transmission line. An example is shown in Figure 3(b), where a two-stage distributed amplifier is depicted. Although the resistive part of the inductors causes an increase in the NF, practical NF values around 3 dB are still achievable in 0.18 μm CMOS [6, 7], similar to those achieved in SiGe BiCMOS technologies [8].

An alternative CMOS LNA topology is presented in [9]. Here a common-gate input stage is loaded with three switched cascode devices with tanks resonating at the center frequency of each of the three bands. Note that the load switching must occur with the same speed as the hopping across the bands, that is, 9.5 ns. Noise figures between 5–7 dB and gains above 20 dB can be obtained.

Current feedback by means of a feedback resistor is also a quite commonly used method to broaden the bandwidth of the input match. In [10] a cascode topology including resistive feedback and a tuned load achieves an NF of 4 dB and a gain of 16 dB in a 0.18 μm CMOS process. Current feedback together with voltage feedback using an integrated transformer is demonstrated in [11]. This LNA (see Figure 4) consists of a cascode input stage (Q1 and Q2), followed by a voltage buffer (Q3 and Q4) known as a white emitter follower. There is voltage feedback by means of a transformer, formed by merging the collector coil and emitter degeneration coil of the input stage. In addition, there is current feedback formed by R1 and C1. This compound feedback mechanism gives high linearity, and also allows for matching of the input impedance to 50 Ω over the lower three bands, without the need for additional external matching components.

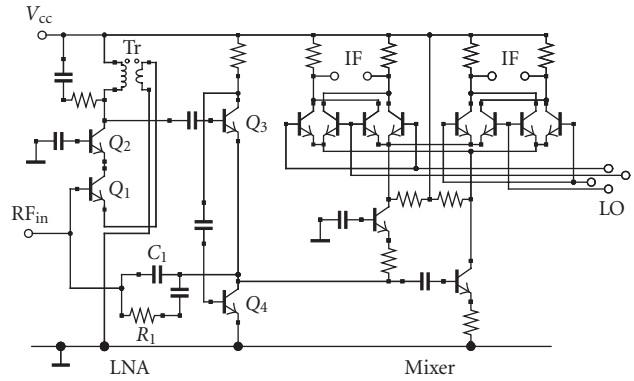


Figure 4: LNA and mixer design.

Due to the channel width of 528 MHz, most receivers apply a zero-IF architecture to relax the bandwidth requirements for the baseband filters and converters. In such an architecture, the LNA is in most cases directly followed by a (Gilbert) down-mixer. In Figure 4, the subsequent mixer contains a combined common-emitter/common-base lower-stage, which is a well-known active balun structure [12]. It is highly degenerated by emitter resistors to obtain the required linearity. A fully balanced eight-transistor switching core has been used, which creates both the I and Q baseband signals. Noise caused by cross-conduction is reduced to a minimum by appropriate shaping of the LO drive signals. These signals should ideally be sinusoidal signals, but as they are the

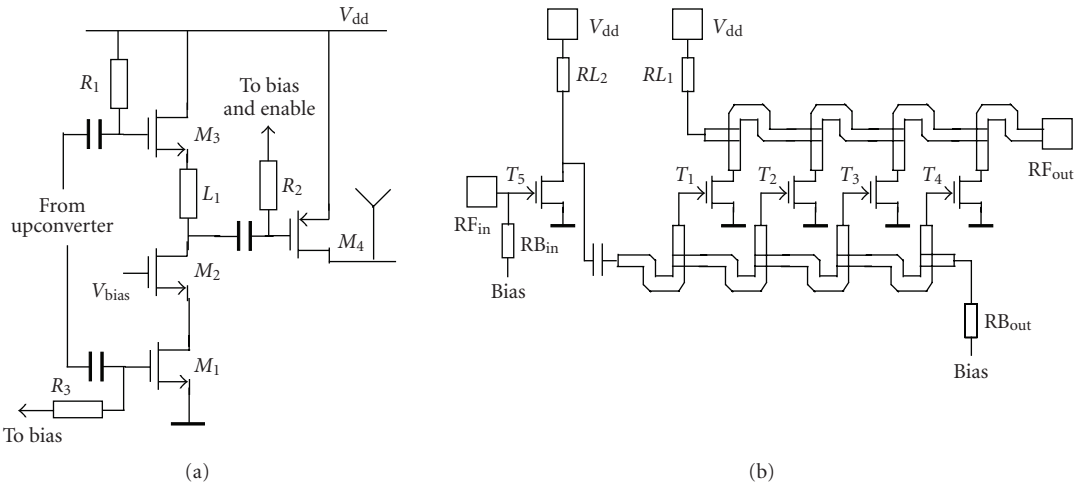


Figure 5: Two implementations of a CMOS RF PA: an inductively loaded PA (a), and a distributed PA (b).

output of frequency dividers, they also contain higher-order harmonics.

A mixer with a variable gain range is demonstrated in [3, 9]. Here, the load resistor is decomposed into binary weighted segments so as to create dB steps in the gain. Implemented in 0.13 μm CMOS, a 30 dB gain is obtained over a large output bandwidth.

High-order filtering at IF/baseband is needed to achieve sufficient attenuation. The large bandwidth in combination with high linearity involves a careful distribution of gain, filtering, and noise. In [11], the baseband filter/VGA has been implemented as a fifth-order Chebyshev-like filter. The gain can be varied between 16 dB and 46 dB with 6 dB steps, and the bandwidth can be tuned in a range of 232 MHz to 254 MHz. At 662 MHz offset an attenuation of -57 dBr has been achieved. A fourth-order Sallen-and-Key filter has been used in [9], while in [13] a fifth-order elliptic filter has been used. In the latter case, the on-chip filter is a passive LC filter and, therefore, it is perfectly linear.

4. RF TRANSMITTER BUILDING BLOCKS

A crucial aspect of a UWB transmitter is the need of power control to ensure that the transmitted level does not exceed the -41.3 dBm/MHz limit (-14 dBm across 528 MHz). Furthermore, as with WLAN systems, RF impairments (e.g., I/Q mismatch, phase noise, carrier feed-through) must be kept to a minimum.

The RF power amplifier (PA) is in most cases based on an inductively loaded (cascode) transistor. An example is shown in Figure 5, where transistors M1 to M3 are used to implement a differential to single-ended structure [9]. Transistor M4 delivers an output level of -10 dBm. A straightforward approach has been used in [14], resulting in a -7 dBm output power level. By varying the bias, the gain of the amplifier can be varied with 6 dB.

Again, also the distributed amplifier has been proposed. In [15] a four-stage amplifier has been implemented in a 0.13 μm CMOS process, resulting in a compression point of +3.5 dBm. In this case the transmission lines are implemented as micro-striplines.

Where in [9] an up-conversion circuit has been used based on resistively degenerated passive mixers along with a current feedback amplifier, two single-side-band Gilbert mixers have been used in [14]. The needed voltage-to-current converter as under stage for the Gilbert mixer core also implements a gain variation mechanism.

5. FAST-HOPPING SYNTHESIZER

A particularly challenging building block of the UWB receiver is the frequency synthesizer. A classical integer-N PLL with programmable loop divider ratio is unable to perform hopping within 9.5 ns, because such a PLL would require a loop bandwidth in the order of at least several hundreds of MHz and a reference frequency of several GHz. The high reference frequency contrasts the frequency resolution of 528 MHz. The high loop bandwidth, apart from being impractical, is in conflict with the phase noise demand [17]. The same argument holds for a fractional-N PLL synthesizer, where the required high loop bandwidth is also hard to combine with the stringent spurious tone demands.

A straightforward frequency synthesizer architecture would be to use three separate PLLs (each generating one of the three required carrier frequencies) in combination with an output multiplexer. This is only practical in those cases where RC ring oscillators can fulfill the requirements. Three LC-oscillators-based PLLs will raise issues with respect to frequency pulling and occupation of die area.The option of using ring oscillators has been used in [9] for a three-band UWB system in a 0.13 μm CMOS process, where each PLL consumes 15 mW from a 1.5 V supply voltage.

Most other proposed synthesizer concepts are based on frequency translation, where two frequencies can be added or subtracted by means of a single-sideband (SSB) mixer

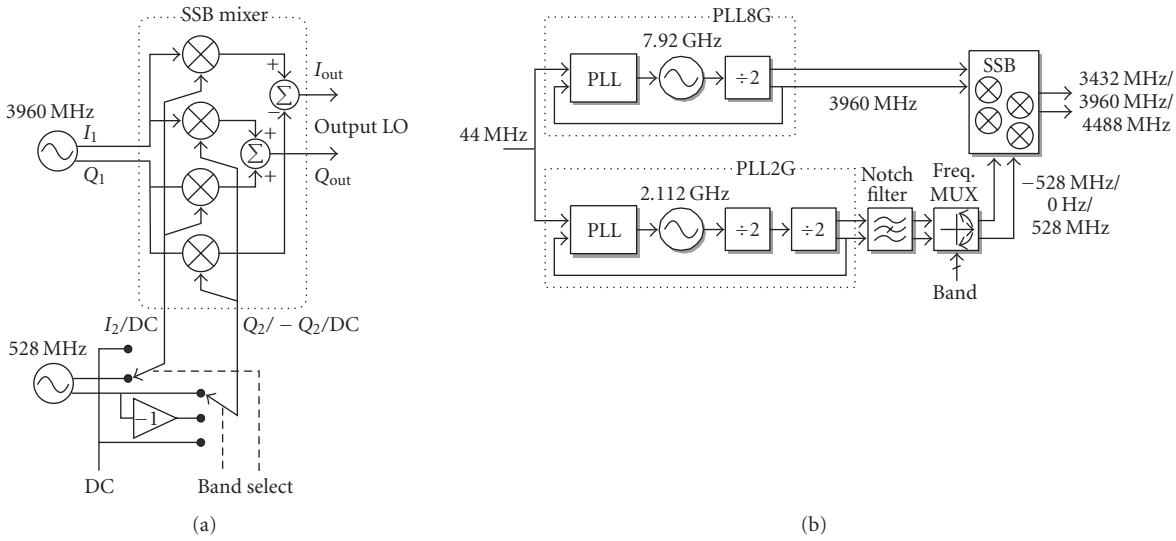


Figure 6: LO scheme based on SSB mixing (a) and a possible implementation (b).

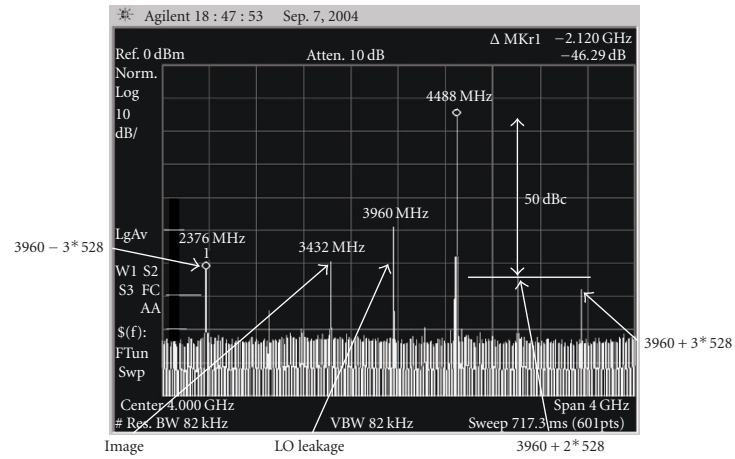


Figure 7: Measured spectral output of the synthesizer in [16] when generating the LO for band #3.

(Figure 6). Synthesizers using this method are also known as multitone generators.

The problem of SSB mixing lies in the inherently generated spurious tones, for example, due to nonlinear behavior of the mixer. In this scheme the third harmonic of the 528 MHz signal (at 1584 MHz) is particularly troublesome because, after mixing with 3960 MHz, this harmonic will cause a spur at either 3960 + 1584 MHz = 5544 MHz or at 3960 − 1584 MHz = 2376 MHz. Both spurs are close to possible strong interferer signals (5 GHz and 2.4 GHz ISM bands, resp.) and this may result in UWB signal corruption. Because the 528 MHz signal is the output of a static divide-by-two circuit in the implementation of Figure 6, its harmonic content will inevitably be strong. Due to the use of quadrature signals, the third harmonic of +528 MHz is located at −1584 MHz. In [16] an integrated notch filter at the divide-by-two output (Figure 5) was used to place a notch at this frequency. In this way, all spurious tones in the 5 GHz band are below −50 dBc, as can be seen from Figure 7. The fully integrated synthesizer consumes 73 mW from a 2.7 V supply and achieves frequency hopping within 1 ns.

To eliminate the need for two PLLs, the 3960 MHz signal needs to be divided by 7.5 to derive a 528 MHz signal. The challenge lies in the design of this divider, especially because of the need for quadrature signals with a 50% duty cycle. In [18] this is accomplished by two modified versions of the Miller divider, one realizing ÷3 and the other ÷2.5. The regenerative loop naturally leads to quadrature outputs and 50% duty cycle. Realized in 0.18 μm CMOS, the image suppression of the divider is −20 dBc while consuming 18 mW from a 1.8 V supply.

One other possibility is demonstrated in [19]. Division by 7.5 has been realized using a frequency divider by 1.5 and a subsequent divider by 5 with postprocessing to make

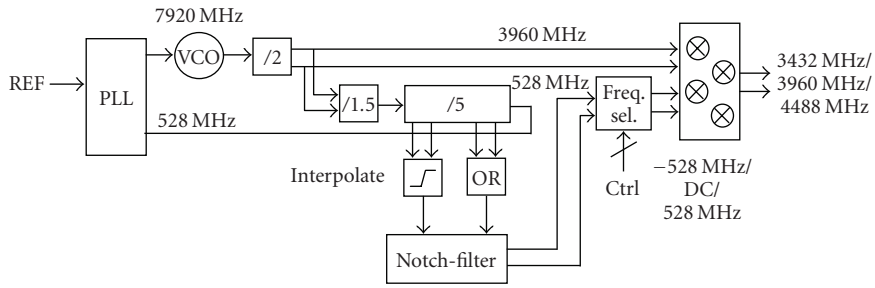


Figure 8: Single PLL, single SSB mixer synthesizer implementation.

clean quadrature signals (Figure 8). The single PLL, single SSB mixer concept consumes 52 mW from a 2.7 V supply. Again due to additional filtering, out-of-band spurious tones are below −50 dBc. The integrated phase noise is below 2 degrees rms and the measured hopping speed is well below the required 9.5 ns.

In literature several proposals have been published in case the higher frequency bands also must be covered. A seven-band synthesizer based on two PLLs and one inductively loaded SSB mixer has been published in [20]. Fabricated in a 0.18 μm CMOS technology, it achieves a sideband rejection of 37 dB. Covering the same bands can also be achieved using a 16 GHz VCO, 2 SSB mixers, and only divide-by-two blocks [13]. A 12-band architecture based on three PLLs and two SSB mixers has been proposed in [3]. Multiplexing and routing of all RF signals will be challenging in this concept.

6. RF TRANSCEIVERS FOR MB-OFDM UWB

As said, due to the wide channel bandwidth, the receiver and transmitter signal paths of UWB systems naturally employ direct conversion, that is, zero-IF. Such a direct conversion 3-band OFDM UWB transceiver has been demonstrated in [9]. The receiver consists of an LNA, quadrature mixers, a fourth-order Sallen-and-Key filter, and a first-order lowpass stage. The LO frequencies are synthesized using three independent PLLs using a 66 MHz reference frequency. This allows a wide PLL loop bandwidth to suppress VCO phase noise. The transmitter uses the inductively loaded PA output stage of Figure 5. It is important to note that the LNA and PA share the same pin connected to the antenna. Designed in a 0.13 μm CMOS technology, this transceiver provides a total gain in the range of 69 to 73 dB and an NF in the range of 5.5 to 8.4 dB across the three bands. The circuit consumes 105 mW from a 1.5 V supply.

A direct conversion architecture for seven-band OFDM UWB has been proposed in [13]. The seven carrier frequencies are generated from a single 16 GHz VCO (see Figure 9). The circuit has been fabricated in a 0.18 μm SiGe BiCMOS process and achieves an NF of 3.3–4.1 dB and a conversion gain of 52 dB. The current consumption is 88 mA from a 2.7 V supply.

A fully integrated receiver front end has been integrated in a SiGe BiCMOS technology with an NPN-f_T of 70 GHz

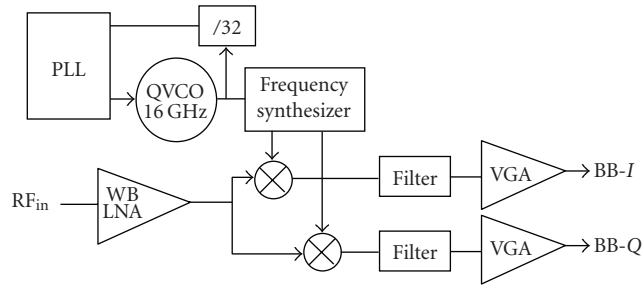


Figure 9: Receiver architecture used in [13]. The PLL is implemented off-chip.

[21]. The block diagram and chip micrograph are shown in Figure 10. The chip with a total area of 4 mm^2 has been packaged in an HVQFN package and mounted on an FR4 board. Digital control blocks for tuning the VCOs and the IF filter as well as a bandgap unit have also been implemented. The measured performance is provided in Table 1 [21], indicating that low noise figures can be achieved for complete receivers. The transmit chain is published in [14] and features wideband elliptic baseband filters, a VGA with dynamic range of 12 dB, an up-conversion mixer, and an RF output stage with a power of −7 dBm. The current consumption is 43 mA at 2.7 V for the complete transmit path.

Finally, some interesting studies on low-power UWB transceiver architectures have been presented in [22, 23]. The architectures are based on the use of distributed design approaches in the LNA and down-mixer circuits.

7. CONCLUDING REMARKS

Several circuit design techniques for multiband UWB have been discussed. Challenging design aspects in UWB are the combination of wideband behavior at radio frequencies and baseband in combination with low noise figures and high linearity, as well as the required fast LO hopping.

Currently most UWB transceivers are realized in a BiCMOS technology. However, recently presented circuit techniques and achievements in CMOS indicate that CMOS transceivers will start competing with their BiCMOS counterparts.

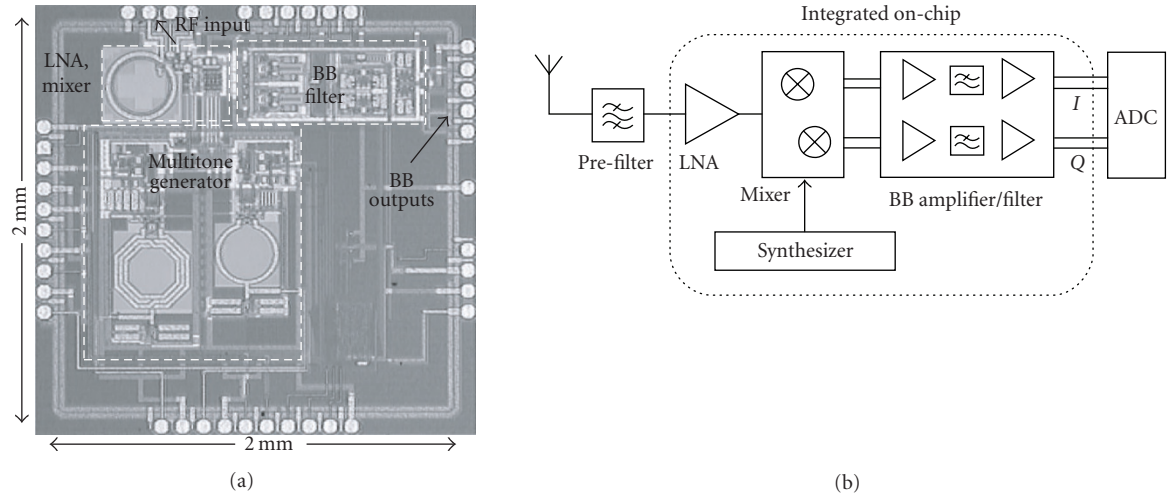


Figure 10: Chip photograph (a) and block diagram (b) of a fully integrated UWB receiver.

Table 1: Measured data of the receiver of Figure 10 (assuming 20 dB attenuation by prefilter).

Parameter	Required	Measured	Info
Current consumption	—	78 mA @ 2.5 V	—
Noise figure	< 6.6 dB[1]	4.5 dB	On PCB, center of IF band, LO is 3960 MHz
Input IP2	> +20 dBm	+25 dBm	f_{in1} : 5 GHz ISM, f_{in2} : GSM1900
Input IP3	> −9 dBm	−6 dBm	f_{in1} : 5 GHz ISM, f_{in2} : 5 GHz ISM
Maximum gain	—	59 dB	Power gain from RF input to base band output
VCO phase noise	< −100 dBc/Hz	−104 dBc/Hz	At 1 MHz offset
Integrated phase noise	< 3.5 degrees rms	1 degrees rms	Integrated from 0 to 50 MHz
In-band spurs	< −30 dBc	< −30 dBc	—
Out-of-band spurs	< −50 dBc	< −50 dBc	For 5 GHz ISM
	< −45 dBc	< −45 dBc	For 2.4 GHz ISM
Hopping speed	< 9.5 ns	< 1 ns	For all allowed hopping sequences

[1] Requirement is < 4.6 dB assuming a pre-filter insertion loss of 2 dB.

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