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CMOS Silicon-on-Sapphire RF Tunable Matching Networks

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This paper describes the design and optimization of an RF tunable network capable of matching highly mismatched loads to 50 Ω at 1.9 GHz. Tuning was achieved using switched capacitors with low-loss, single-transistor switches. Simulations show that the performance of the matching network depends strongly on the switch performances and on the inductor losses. A 0.5 μm silicon-on-sapphire (SOS) CMOS technology was chosen for network implementation because of the relatively high-quality monolithic inductors achievable in the process. The matching network provides very good matching for inductive loads, and acceptable matching for highly capacitive loads. A 1 dB compression point greater than +15 dBm was obtained for a wide range of load impedances.

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1. INTRODUCTION

Matching impedance networks have become ubiquitous in all radio-frequency (RF) transmitters and receivers, especially in wireless mobile devices such as handheld computers (PDs) and cellular phones. Fixed matching networks are inserted between the power amplifier (PA) module and the antenna. However, antenna input impedance is affected by the presence of surrounding objects [1–4], and can vary considerably with the antenna close to the human body or with the position of the hand on a handset. The few published measurements of those variations showed a mismatch that can cause more than half of the transmitted power to be reflected [5]. When that mismatch occurs between the antenna and the PA, the radiated power efficiency decreases, increasing the demand on the battery. To address this issue, tunable matching networks have been considered by researchers in recent times [6–9]. Such circuits, known as antenna tuning units (ATUs), can be realized using tuned L-match, T-match, or Π-match (or a cascade of many sections of them) sections whose components can be controlled electronically through different algorithms such as the genetic algorithm, or simulated annealing.

RF MEMS-based matching networks have been the subject of substantive efforts for the last decade [10]. However, their use remains limited to microwave and high-frequency applications (above 20 GHz). Issues of reliability, actuation voltage, and packaging prevent their acceptance in commercial applications. Recently, an RF MEMS impedance tuner at 6–20 GHz was fabricated [11], but its impedance matching region at 6 GHz was limited. Recent advancements in CMOS-based IC technology have made it, arguably, the main contender for volume wireless products. A CMOS-based ATU was recently studied [12], demonstrating promising performance.

In this work, the design and simulation results of different switching topologies using a commercial 0.5 μm silicon-on-sapphire (SOS) UTSi technology [13] at 1.9 GHz are described. We analyze our results primarily in terms of S21 parameters, as S21 encompasses both the reflection loss and the loss in the matching network.

An optimized switch circuit is used to design switched-capacitor-based matching networks for 1.9 GHz operation, dedicated to matching loads within the voltage standing wave ratio (VSWR) circle of 5.6. It should be noted that the fabrication process provided transistors with constant widths and variable lengths. The transistor used in this work is an n-channel FET whose length can vary between 0.5 and 1 μm, and its finger width is fixed at 18 μm. The number of fingers ranges from 3 to 61 for this type of device. Furthermore, the SOS MOSFETs are different from bulk MOSFETs in that there is no substrate connection. In the commercial design kit used in this work, the device model P-channel body (NMOS) is tied to −50 V in order to avoid forward biasing the junction diodes under all signal conditions.

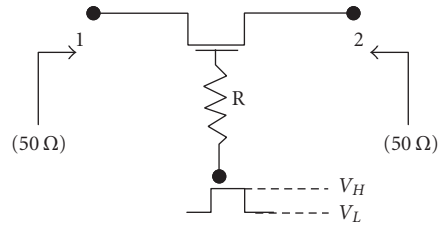

Figure 1: Single-transistor switch.

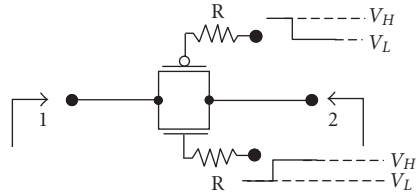

Figure 2: The transmission gate.

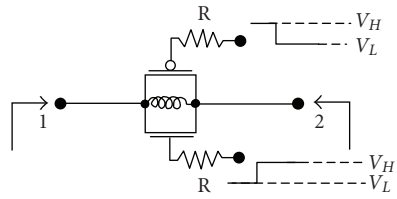

Figure 3: The resonant transmission gate (TG_Res).

2. RF SWITCH

Switches used in digital and low-frequency applications are usually characterized by their switching time and input capacitances. In RF applications, however, these metrics may not be adequate to describe their real properties. Instead, three parameters are commonly scrutinized before choosing a switch: the losses in ON and OFF states, known as insertion loss (IL) and isolation (ISO), respectively, and the linearity of the switch specified by its 1 dB compression point in the ON state. IL and ISO are obtained when the switch is connected in series with a 50 Ω RF source and a 50 Ω load resistance. A good switch should present low loss, high linearity, and high isolation. Hence, optimization must account for both ON and OFF states of the switch.

The next subsections compare different switching circuits and select the one having the best tradeoff of IL, ISO, and linearity. All simulations and optimizations were performed using Agilent-ADS software, using the technology file provided by the process manufacturer.

2.1. Single-transistor switch

A single-transistor switch (STS) represents the simplest switching topology, as shown in Figure 1. NMOS is usually used rather than PMOS since the NMOS has larger transconductance and higher electron mobility. In this circuit, the drain and source are biased equally by 0 V through bias resistors of 10 kΩ (not shown in the schematic). The control voltage is applied to the gate through a 10 kΩ resistor as well with values of +3 V (ON state) and −1 V (OFF state). These values can be adjusted upward or downward to accommodate a required dc signal path bias, or to avoid the negative supply.

2.2. Transmission gate switch

The drawback of the STS is its increased nonlinearity with increased signal power. This is due to the dependency of the on-resistance on the input voltage amplitude. The transmission gate (TG) shown in Figure 2 accommodates greater voltage swings because the on-resistance is relatively signal-independent. However, such a switch requires complementary clocks to turn the transistors ON or OFF simultaneously. In this circuit, the drains and sources are biased equally by 0 V through bias resistors of 10 kΩ (not shown in the schematic). The high (3 V) and low (−1 V) control voltages are applied to the gates through 10 kΩ resistors.

2.3. The resonant transmission gate (TG_Res)

An efficient way to improve the isolation of the TG switch consists of adding a shunt inductor that resonates with the off-state parasitic capacitances as shown in Figure 3. The value of the inductor is calculated based on the value of the off-state capacitances at the operating frequency $\omega_0 = (\sqrt{L \cdot C})^{-1}$, where C is the off-state capacitance of the switch.

2.4. The LC-resonance switch

The LC-resonance switch depicted in Figure 4 was first suggested in [14]. In the OFF-mode, transistors M1 and M2 are ON, which will cause a parallel resonance formed by L and C_1 that will isolate the signal. In the ON-mode, M1 and M2 are OFF, and a series resonance occurs through the L-C_2 path that will allow the signal to pass.

Figure 5 shows the insertion loss and isolation of the four different switching topologies as a function of the number of fingers (nf) of the transistors. Table 1 summarizes the best tradeoff between IL and ISO of these switches.

The TG and TG_Res have the same IL. However, TG_Res achieves a much better isolation. When both NMOS and PMOS transistors have 36 fingers, the required value of the resonance inductor is then 11.54 nH at 1.9 GHz. The quality factor (Q) of the inductor is 20, which is available in the SOS fabrication process.

The behavior of the LC_resonance switch depends on the quality factor of the inductor. The best tradeoff between its IL and ISO was obtained for a number of fingers of 61, for both M1 and M2. The inductor value necessary to resonate with C1 at 1.9 GHz is 3.2 nH ($Q = 20$), and C1 = C2 = 2.2 pF.

3. SWITCH ANALYSIS

The target matching network will use banks of parallel switched capacitors connected to ground through grounded

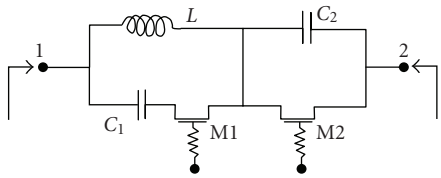

Figure 4: The LC-resonance switch.

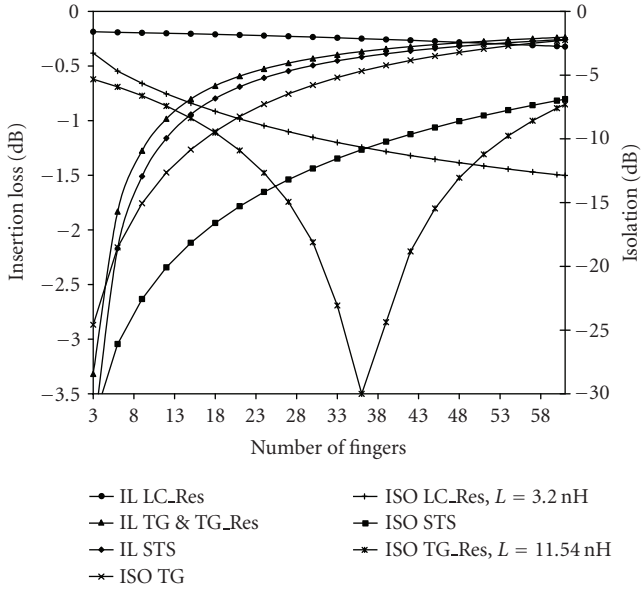

Figure 5: IL and ISO of all the switches, the technology limits the number of fingers to 61.

Table 1: Optimal IL and ISO of the different switching topologies.

	IL (dB)	ISO (dB)
STS (nf = 36)	−0.5	−11
TG (nf = 36)	−0.36	−5
TG_Res (nf = 36)	−0.36	−30
LC_resonance (nf = 61)	−0.32	−13

switches, in conjunction with inductors in various configurations. This topology has shown the best performance, as previously described [11]. It is important to select a switch that presents a low on-resistance and low off-capacitances to maximize the performance of the final network.

In the next subsections, we will examine the behavior of grounded switches and their power handling capabilities in order to select the most suitable switching topology for the application.

3.1. Source-grounded switch

Figure 6 shows the source-grounded switch configuration.

Table 2 shows the input impedances and the capacitances of the switches in their off-states. The table also provides the number of fingers of the transistors used. The parasitic

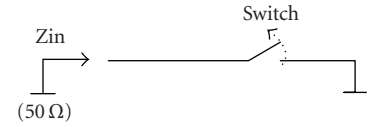

Figure 6: Source-grounded switch configuration.

Table 2: Off-state input impedances of the switches when sources are grounded.

	Zin (OFF)	Real (Zin)	C_{in} (OFF)
STS (nf = 36)	2.7–j*333	2.7	0.25 pF
TG (nf = 36)	0.95–j*138	0.95	0.6 pF
TG_Res (nf = 36)	880–j*1160	880	72 fF
LC_resonance (nf = 61)	336–j*16	336	5 pF

Table 3: Summary of the switches maximum incident power handling performances.

	50 Ω		Grounded source	
	ON state	OFF state	ON state	OFF state
STS (nf = 36)	25 dBm	22.5 dBm	19.5 dBm	19.5 dBm
TG (nf = 36)	26.5 dBm	2 dBm	21 dBm	0 dBm
TG_Res (nf = 36)	26.5 dBm	0 dBm	22 dBm	0 dBm
LC_resonance (nf = 61)	24.5 dBm	23.5 dBm	19 dBm	22 dBm

element that most significantly affects the operation of a bank of parallel switched capacitors is the parasitic off-state capacitance of the switch, which reduces its isolation. It can be seen that the STS and the resonant TG provide the lowest off-state capacitances. The STS has a lower parasitic resistance, whereas the resonant TG presents a higher value.

3.2. Switch reliability: power handling

Reliability of the switch needs to be examined in the presence of a large RF input signal in combination with the output mismatch. Under these conditions, it is important to make sure that the switch is working below the maximum acceptable voltage drop across the gate oxide, which is 3.3 V in the process studied in this work. Table 3 summarizes the maximum incident power handling capability of the different switches either terminated in 50 Ω or grounded in ON and OFF states.

The switch 1 dB compression point was also examined. Here, a major difference appears between bulk and SOS transistor technology. In a bulk MOSFET process, a switch starts compressing when an applied RF input signal is large enough to make the source/drain-to-body junctions forward biased in some portion of a cycle. A second mechanism occurs when the source is grounded and the switch is OFF. The drain voltage capacitively couples into the gate causing V_{GS} to momentarily exceed the threshold voltage. This will result in channel conduction for a portion of the drain cycle. The first phenomenon does not exist in SOS technology because the bulk is isolated. It is only the second phenomenon that may

take place when the switch is OFF. This has indeed been observed in simulations with the STS switch, which only compresses in its OFF state showing a $P_{1\,dB}$ of +15 dBm in 50 Ω and ground terminations.

From the above results, we can deduce that the STS presents the best tradeoff between IL and ISO for 50 Ω and grounded source configurations, while providing fairly good power handling. The STS and LC-resonance configurations have comparable power handling performance. However, the STS uses less elements and is less sensitive to frequency variations. As a result, the STS is selected as the switch in the matching networks described in the next sections.

4. MATCHING NETWORKS

We first examine capacitor banks, which will form a major part of a complete matching network.

A bank of four parallel capacitors connected to ground through four different sets of switches, all switched OFF, was simulated as shown in Figure 7(a). When the switches are turned off, the insertion loss (S21) between ports 1 and 2 should be very low. Figure 7(b) is another topology that loads the through line with only two capacitive branches, instead of four, as in Figure 7(a). This new topology provides the same selection of capacitance values as does the circuit of Figure 7(a). Figure 7(c) shows the simulated insertion loss of the two circuits with the dimensions given in Table 2.

Figure 7(c) shows that the topology that presents the least effect on the thru line is that of Figure 7(b). This is an expected result since it loads the line with less elements than does the first topology. The TG switch was not included in the simulation because of its bad isolation.

Now that the behavior of the individual switched capacitor banks has been examined, we consider a complete matching network. The simplest type of reactive matching network is the L-section [15]. The L-section allows two degrees of freedom among three specifications: centre frequency, impedance transformation (load/source impedances), and network Q (or bandwidth). Once impedance transformation and center frequency are specified, Q (or bandwidth) is automatically determined. Π (Pi) and T-match networks present more flexibility whereby one can independently specify center frequency, Q, and the impedance transformation ratio [16]. A Π-match can be considered as a cascade of two L-sections, and they lead to the same matching properties [17–20]. The next subsections will focus on the design of ideal and real Π-matching networks to match loads having high VSWR.

4.1. *Ideal* Π*-matching network*

Figure 8(a) shows the target impedance locations to be matched by the matching network. These impedances Z_L are located on the circle which represents a VSWR of 5.6, and are defined as

$$Z_L = 50 \cdot \frac{1 + |\rho| e^{j\phi}}{1 - |\rho| e^{j\phi}}, \tag{1}$$

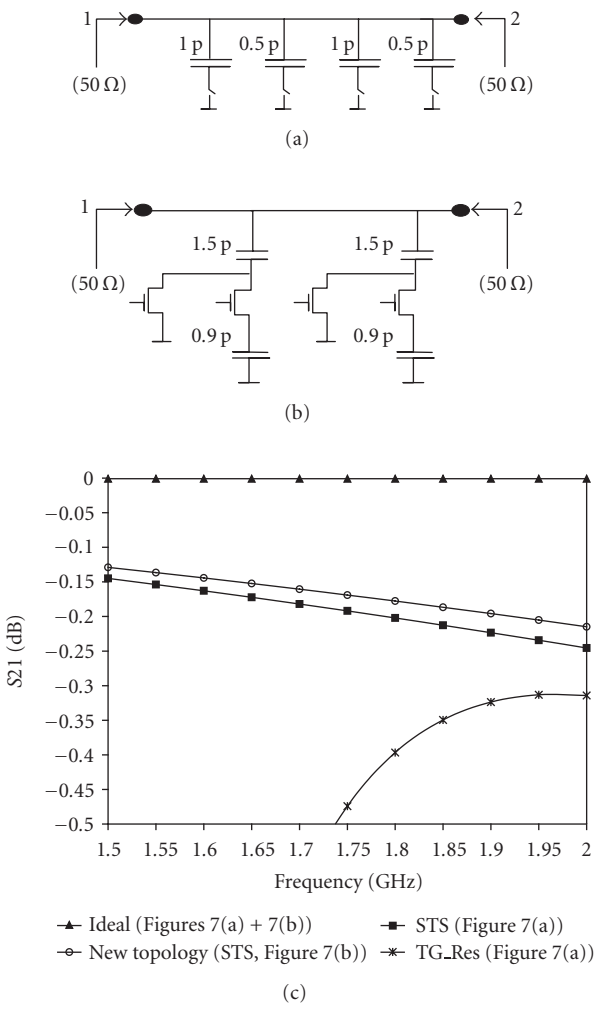

Figure 7: (a) A bank of 4 parallel capacitors, (b) new topology, and (c) simulation results.

where $|\rho|$ is the magnitude of the reflection coefficient, and ϕ is its angle (in rad or its equivalent in degrees $-180 < \phi < 180$). VSWR of 5.6 is equivalent to a reflection coefficient $|\rho|$ of 0.7 (S11 = S21 = −3 dB), and it encompasses a wide range of mismatched loads in a practical circuit. The Π-matching network topology is shown in Figure 8(b). It uses one fixed inductor of 3.2 nH, and two banks of four switched capacitors. To begin the discussion, all components are assumed to be ideal, and the switches are controlled independently. The elements of each capacitor bank are arranged in a binary array, and the discrete capacitive values of each capacitor bank may be expressed as

$$C_{L,R} = (a_1 2^0 + a_2 2^1 + a_3 2^2 + a_4 2^3) C_{min}, \tag{2}$$

where C_L and C_R are left- and right-hand side capacitor bank values, respectively, and C_{min} is the minimum value of each capacitor bank. The coefficients a_1 to a_4 are either 0 when a switch is OFF, or 1 when a switch is ON. The maximum and

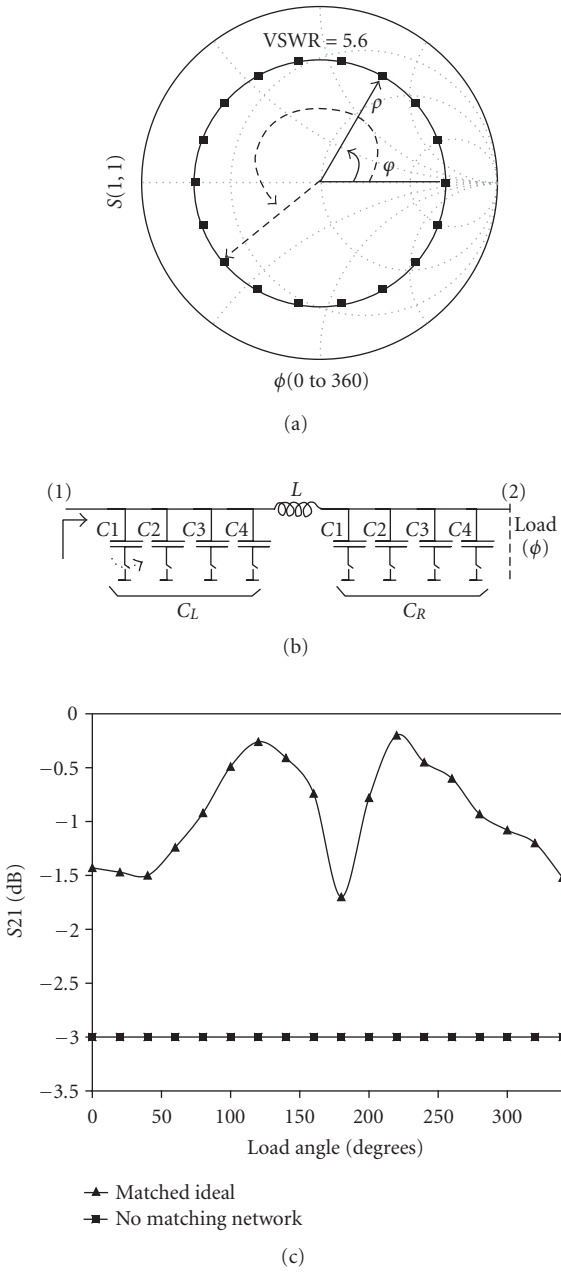

Figure 8: (a) Circle of load impedances of VSWR of 5.6; (b) ideal Π-matching network; and (c) the insertion losses obtained before and after matching of loads located on the circle circumference (S11 = S21 = −3 dB).

minimum capacitance values of each bank can be related as

$$\frac{C_{Lmax,Rmax}}{C_{min}} = 2^n - 1 = 15, \quad (3)$$

where n is the number of switched capacitors of each bank. We choose a realistic value for $C_{min} = 0.5$ pF (or C1). Thus, C2 = 1 pF, C3 = 2 pF, and C4 = 4 pF.

Figure 8(c) shows the simulated insertion losses obtained with and without matching with the ideal Π-matching network. The simulated load impedances are located on the VSWR circle of 5.6, separated evenly by $\pi/9$ rad (phi = 20 degrees). This result shows the best matching that can be obtained with this 1-Π circuit. The effect of the use of real components on this result will be highlighted in the next subsections.

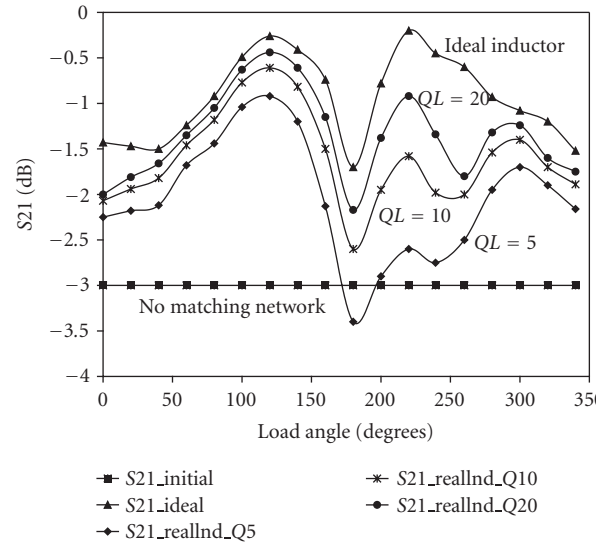

Figure 9: Comparison of insertion losses obtained with ideal and real inductors with different Q values. The switches are ideal in all cases.

4.2. *Real* Π*-matching network*

This section shows how the matching network performs when realistic rather than ideal inductors and switches are used.

4.2.1. *Real inductor and ideal switches*

First, the effect of a real inductor will be investigated. Its value used in this Π-match is 3.2 nH at 1.9 GHz operation. Replacing the ideal inductor with realistic inductors with $Q = 5, 10$, and 20, respectively, leads to the result displayed in Figure 9. Note that Q of 20 is close to the value achievable in the chosen SOS process. The capacitors used here are MIMCAPS whose quality factor is higher than 100, however, the switches are still ideal. It can be seen that despite the use of a real inductor, the matching does not deteriorate considerably, and the result remains acceptable provided the inductor is not highly lossy.

4.2.2. *Ideal inductor and real switches*

The matching behavior was then investigated using real switches. The inductor is ideal in order to only assess the effect of the switches. The final result is shown in Figure 10. Again, the TG switch was not simulated in this case because of its bad isolation.

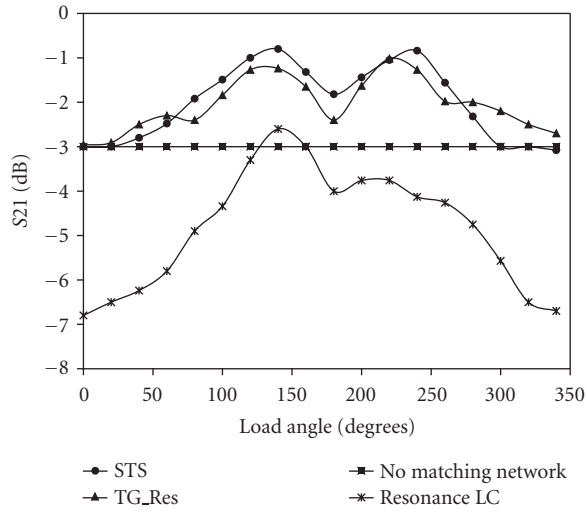

Figure 10: Comparison of insertion losses obtained with different real switches and ideal inductor.

It is clear that the resonance-LC switch adds huge parasitic capacitances (as shown in Table 2) and thus cannot be used. The resonant TG switch shows good performance, but its low-power capability keeps it from being used for high-power signals. On the other hand, the single-transistor switch (STS) has a good matching potential as well as a good power-handling capability as shown previously. Therefore, the STS is selected for the matching network. The combined effects of nonideal switches and inductors will be discussed in the next sections.

5. 2-Π MATCHING NETWORK

It is apparent from the previous section that a 1-Π network does not significantly improve the match for some loads. Cascading two 1-Π matching networks may provide the required latitude in circuit parameters to acceptably match a wider range of impedances. The next subsections will introduce a 2-Π matching network with ideal as well as realistic components.

5.1. *Ideal 2-Π matching network*

Figure 11(a) shows a 2-Π matching network, which uses 2 inductors and 3 banks of switched capacitors. In this example, all components are assumed to be ideal, and the 10 switches are controlled independently. The inductors used are L1 = 4.2 nH and L2 = 3.2 nH. This network uses the same capacitor bank topology used in the previous case. The capacitor values are C1 = 0.5 pF, C2 = 1 pF, C3 = 2 pF, and C4 = 4 pF.

Figure 11(b) shows the simulated insertion losses obtained with and without matching with the ideal 2-Π matching network. Again, the load impedances are located on the VSWR circle of 5.6, separated evenly by $\pi/9$ rad (phi = 20 degrees). This result shows that excellent matching can be

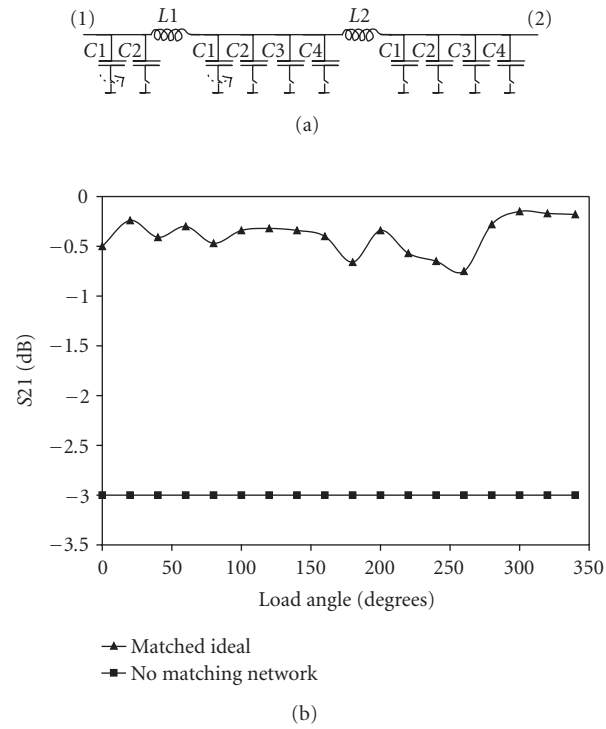

Figure 11: (a) Ideal 2-Π matching network and (b) the insertion losses obtained before and after matching a load with a VSWR of 5.6 (S11 = S21 = −3 dB).

obtained with a 2-Π matching network. The effect of the use of real components on the circuit will be pointed out in the next subsections.

5.2. *Real 2-Π matching network*

Figure 12 shows the insertion losses obtained with the 2-Π matching network using (1) real inductors (Q = 20) and ideal switches, (2) real switches and ideal inductors, and (3) real inductors and switches. The capacitors are MIMCAPS, and the transistor switches are controlled independently by digital signals of amplitudes of −1 V (OFF state) and +3 V (ON state). Drains and sources of the switches are biased by 0 V through 10 kΩ resistors (not shown in the figure).

It can be seen from the figure that the effect of the switches is greater than that of the inductors. Furthermore, it is observed that both switch and inductor losses lead to significantly reduced matching performance with capacitive loads. Hence, it is expected that introduction of a phase shifter in front of the matching circuits can improve overall system performance.

5.3. *2-Π matching network with phase shifter*

A tunable phase shifter was then designed to shift the capacitive load phases for a maximum phase shift of 100 degrees. The phase shifter shown in Figure 13(a) [21, 22] presents a maximum phase shift of 80 degrees when its input and

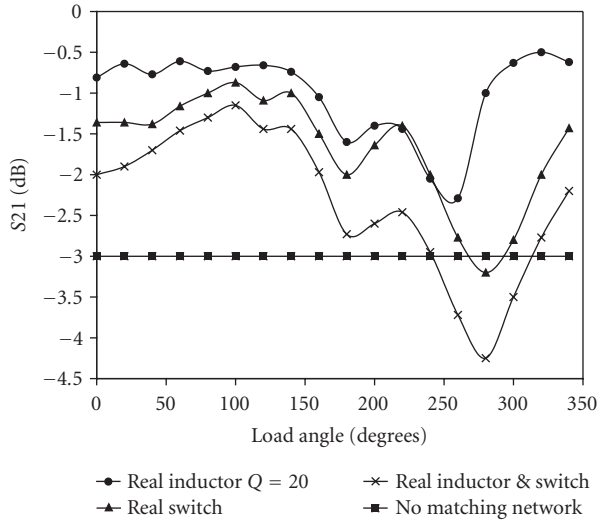

Figure 12: Comparison of insertion losses obtained with real inductors ($Q = 20$), real switches, and real switches and inductors. Loads have VSWR = 5.6.

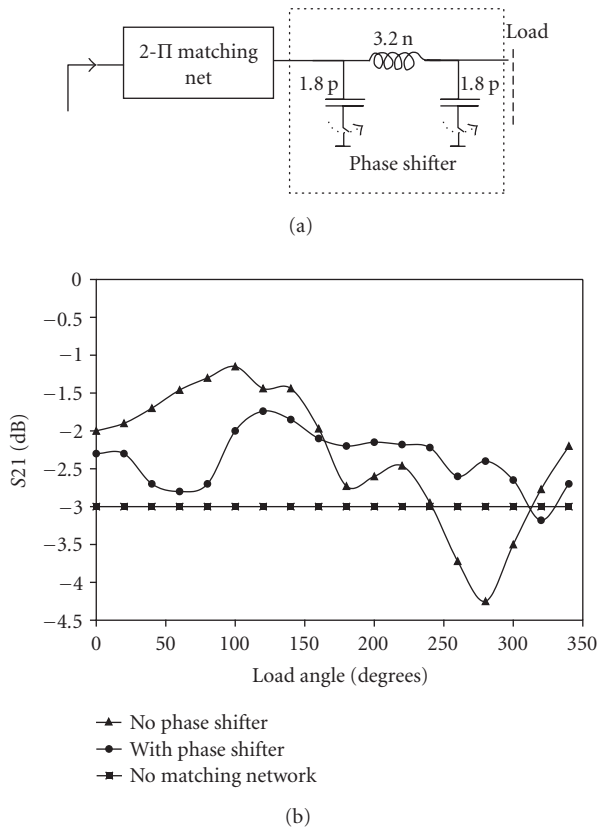

Figure 13: (a) 2-Π matching network followed by a tunable phase shifter; (b) insertion losses of the 2-Π matching network with and without phase shifter. All components are realistic.

output ports are terminated in 50 Ω. However, this phase shift becomes as high as 120 degrees when its output port is mismatched.

While one can argue that this phase shifter is nothing but another Π-matching network, the circuit has been designed separately to provide the required phase shift.

Figure 13(b) shows the insertion loss of the 2-Π matching network with and without the phase shifter. The matching network and phase shifter use real components with all inductors assumed to have Q of 20. It can be seen that the mismatch in the capacitive zone has been reduced and all capacitive loads, but one, have their matching conditions improved.

Note that the capacitor banks used so far are the ones of the topology of Figure 7(a). However, it has been demonstrated that switched capacitors of Figure 7(b) have less parasitic effects on the signal carried on the through line. Consequently, this new topology has been examined on the 2-Π matching network.

5.4. New 2-Π match core

The new 2-Π matching network topology is depicted in Figure 14(a). It uses three capacitor banks and two inductors, the same as the circuit of Figure 11(a). The first capacitor bank provides two different capacitive loads of C1 = 1.5 pF (switch S1 is ON and S2 is OFF) and C1//C2 = 0.56 pF (S1 is OFF and S2 is ON). The middle capacitor bank provides four capacitive loads controlled in a similar way as the first bank, as does the third bank. Figure 14(b) shows the schematic of the real matching circuitry (bias network not shown). The component values are C1 = C3 = C7 = 1.5 pF; C2 = C4 = C8 = 0.9 pF; C5 = C9 = 1 pF; C6 = C10 = 20 pF (used as decoupling capacitors). The values of inductors L1 and L2 are 4.2 nH and 3.8 nH, respectively, with a Q of 20 for both. The STS characteristics are given in Table 2. The simulated insertion loss obtained with this topology is shown in Figure 14(c).

This new topology is capable of providing a good matching for inductive loads, but unacceptable matching for capacitive loads. Using a variable phase shifter should address this shortcoming.

5.5. New 2-Π match core with phase shifter

The new 2-Π matching network was then augmented with a tunable phase shifter, as shown in Figure 15(a). The characteristics of this phase shifter are similar to the ones in the previous section. It provides a maximum phase shift of 80 degrees when terminated with 50 Ω. However, this phase shift increases when one of its port impedances is different from 50 Ω. This phase shifter uses two capacitor banks controlled by single-transistor switches (STS). The inductor Q is also 20. The resulting insertion loss of the whole circuit is shown in Figure 15(b).

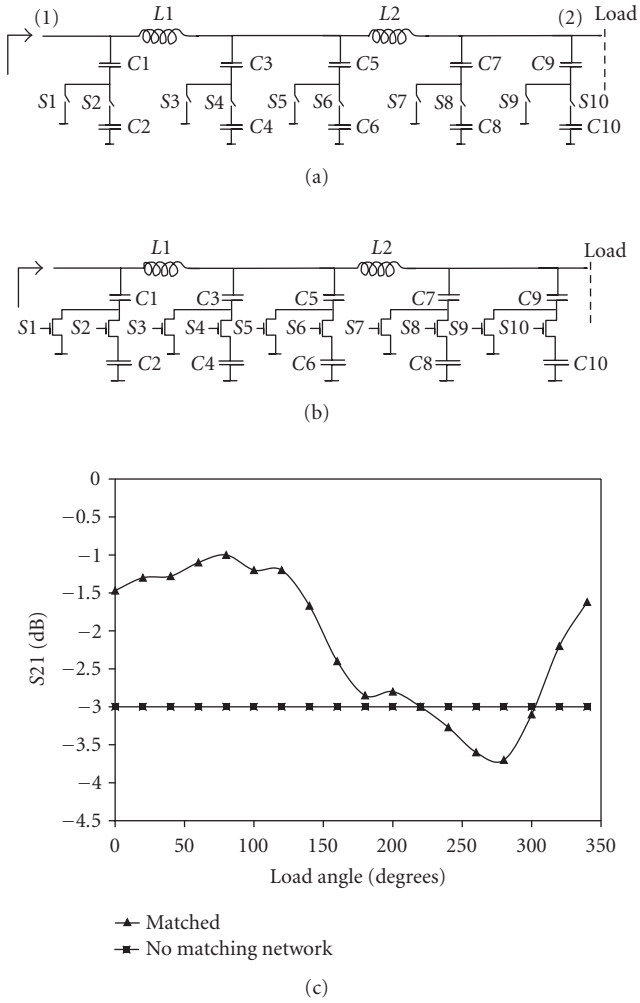

FIGURE 14: (a) and (b) 2-Π matching network using the new capacitor bank topology; (c) simulated insertion loss. All components are real.

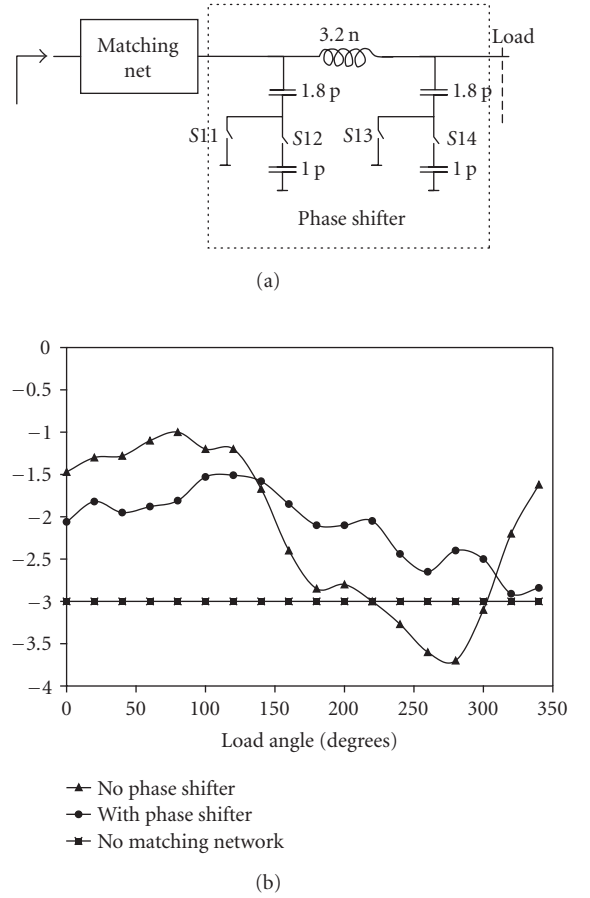

FIGURE 15: (a) The new 2-Π matching network followed by a tunable phase shifter; (b) insertion losses of the 2-Π matching network with and without phase shifter.

5.6. Optimization of the new 2-Π matching network

The matching network of Figure 15(a) was further optimized in order to improve its matching capability for capacitive loads. This has been done through the following procedure: given that each load impedance is matched by finding the right combination of switch states, there are then X switches ON and (N–X) switches OFF for each load where N is the number of switches of the network. In the example being discussed, N = 14 with the phase shifter included (Figures 13(a) and 14(a)). Then, those (N–X) switches (which are OFF) have been compared for each load and it has been observed that switches 5, 7, and 9 of Figure 14(a) are ON for only one time for all load impedances. Consequently, removing those three switches, as shown in Figure 16(a), and comparing the new insertion loss with the one of Figure 15(a), we obtain the result displayed in Figure 16(b).

The final result shows improvement in the general behavior of the matching network with highly capacitive loads.

5.7. Matching different loads

The optimized new matching network has been examined to match heavily mismatched loads. The result is shown in Figure 17 for loads having VSWR of 9 ($|\rho| = 0.8$; S21 = −4.4 dB), and 12.3 ($|\rho| = 0.85$; S21 = −5.5 dB). The result shows improvement in their matching behavior, even though capacitive loads are not as well matched as inductive loads.

It should be noted that when the network is actually matched, that is, the load is 50 Ω, the network's simulated insertion loss is 1 dB. This mismatch is due to the presence of the three inductors of the network between the generator and the 50 Ω load, and switches S6 and S8 are ON to compensate for their effects. Consequently, the system VSWRs will always be greater than or equal to 2.5. However, at the same time, large improvements in the match are seen for significantly mismatched networks, improving the overall power savings.

6. POWER CAPABILITY OF THE OPTIMIZED NETWORK

Figure 18 shows the simulation results of the insertion loss and power capability of the optimized new 2-Π matching

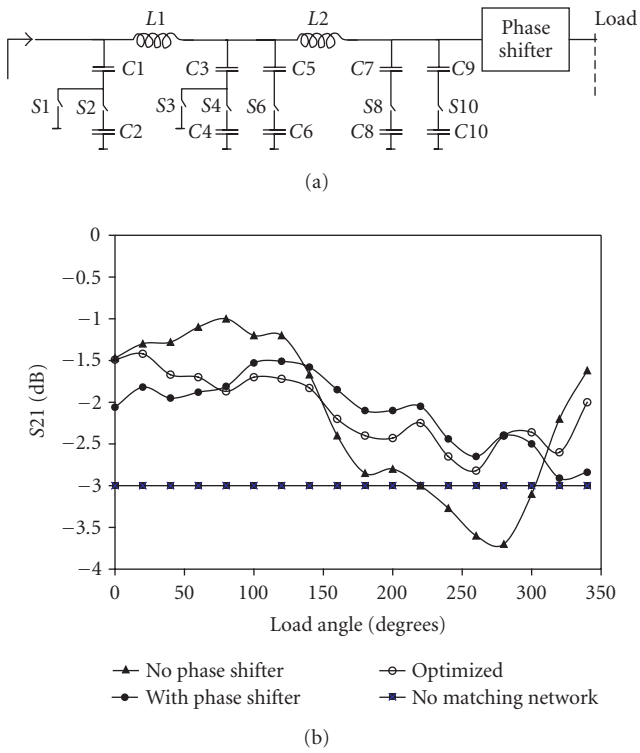

Figure 16: (a) The optimized new 2-Π matching network followed by a tunable phase shifter; (b) insertion losses of the 2-Π matching network with and without phase shifter.

network shown in Figure 16(a) at 1.9 GHz for load impedances with VSWR of 5.6, separated evenly by $\pi/9$ rad (phi = 20 degrees).

The result shows 1 dB compression points that vary with the load values. The power handling capability is quite good over the entire range of load impedances.

7. CONCLUSION

The design and optimization of matching networks in an SOS CMOS process have been presented in this paper. Different switching components have been described. The ability of the networks to match loads depends strongly on the Q factor of the inductors used as well as IL and ISO of the switches. The selected single-transistor switch (STS) topology is capable of handling signal power as high as +20 dBm. The goal of matching highly mismatched loads with VSWR > 5.6 required the cascade of two Π matching networks with a phase shifter. The final network configuration was capable of matching a wide range of inductive and capacitive loads.

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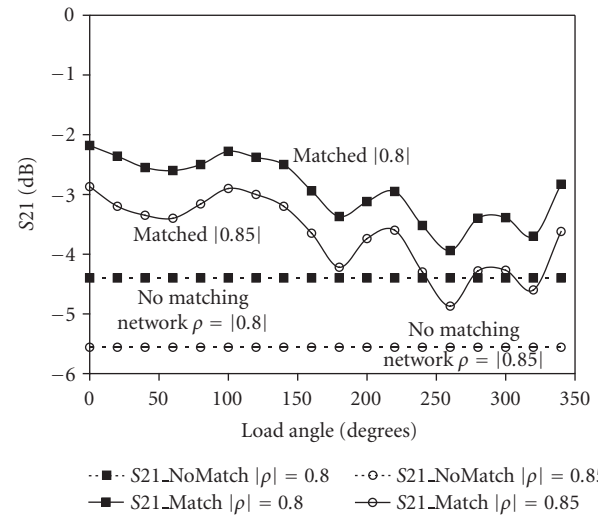

Figure 17: Insertion loss obtained with the optimized new 2-Π matching network for load having reflection coefficients of 0.8 and 0.85.

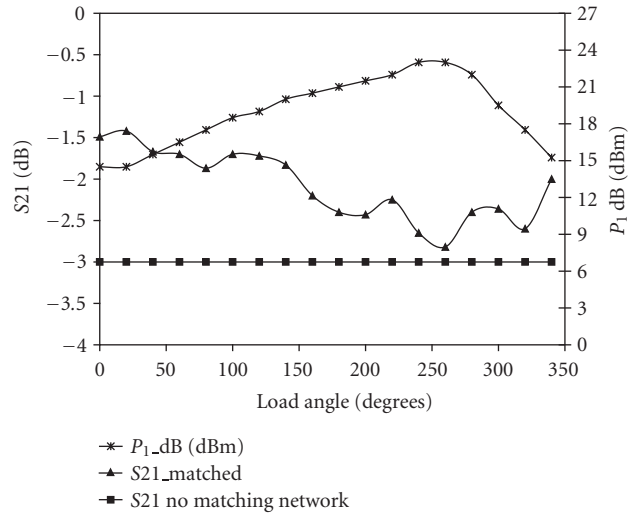

Figure 18: Insertion loss and the 1 dB compression points obtained with the optimized new 2-Π matching network for loads having a reflection coefficient of 0.7.

REFERENCES

[1] K. Karimullah, D. Nyquist, and K. Chen, "Interaction of thin-wire antennas with conducting, polarizable bodies—theory and experiment," in *Proceedings of IEEE International Symposium on Antennas and Propagation Society (APS '78)*, vol. 16, pp. 219–222, College Park, Md, USA, May 1978.

[2] O. Norklit, P. D. Teal, and R. G. Vaughan, "Measurement and evaluation of multi-antenna handsets in indoor mobile communication," *IEEE Transactions on Antennas and Propagation*, vol. 49, no. 3, pp. 429–437, 2001.

[3] M. A. Jensen and Y. Rahmat-Samii, "Performance analysis of antennas for hand-held transceivers using FDTD," *IEEE Transactions on Antennas and Propagation*, vol. 42, no. 8, pp. 1106–1113, 1994.

[4] J. Toftgard, S. N. Hornsleth, and J. B. Andersen, "Effects on portable antennas of the presence of a person," *IEEE Transactions on Antennas and Propagation*, vol. 41, no. 6, pp. 739–746, 1993.

[5] J. de Mingo, A. Valdovinos, A. Crespo, D. Navarro, and P. Garcia, "An RF electronically controlled impedance tuning network design and its application to an antenna input impedance automatic matching system," *IEEE Transactions on Microwave Theory and Techniques*, vol. 52, no. 2, pp. 489–497, 2004.

[6] L.-Y. Vicki Chen, R. Forse, D. Chase, and R. A. York, "Analog tunable matching network using integrated thin-film BST capacitors," in *IEEE MTT-S International Microwave Symposium Digest*, vol. 1, pp. 261–264, Fort Worth, Tex, USA, June 2004.

[7] J. R. Moritz and Y. Sun, "Frequency agile antenna tuning and matching," in *Proceedings of 8th International Conference on HF Radio Systems and Techniques (IEE Conf. Publ. No. 474)*, pp. 169–174, Guildford, UK, July 2000.

[8] D. M. W. Leenaerts, "Low power RF IC design for wireless communication," in *Proceedings of International Symposium on Low Power Electronics and Design*, pp. 428–433, Seoul, Korea, August 2003.

[9] A. A. Abidi, "Low-power radio-frequency IC's for portable communications," *Proceedings of the IEEE*, vol. 83, no. 4, pp. 544–569, 1995.

[10] T. Vaha-Heikkila, J. Varis, J. Tuovinen, and G. M. Rebeiz, "A 20-50 GHz RF MEMS single-stub impedance tuner," *IEEE Microwave and Wireless Components Letters*, vol. 15, no. 4, pp. 205–207, 2005.

[11] T. Vaha-Heikkila, J. Varis, J. Tuovinen, and G. M. Rebeiz, "A reconfigurable 6-20 GHz RF MEMS impedance tuner," in *IEEE MTT-S International Microwave Symposium Digest*, vol. 2, pp. 729–732, Fort Worth, Tex, USA, June 2004.

[12] P. Sjoblom and H. Sjoland, "An adaptive impedance tuning CMOS circuit for ISM 2.4-GHz band," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 52, no. 6, pp. 1115–1124, 2005.

[13] Peregrine website: http://www.psemi.com.

[14] T. Tokumitsu, I. Toyoda, and M. Aikawa, "A low-voltage, high-power T/R-switch MMIC using LC resonators," *IEEE Transactions on Microwave Theory and Techniques*, vol. 43, no. 5, pp. 997–1003, 1995.

[15] C. Bowick, *RF Circuit Design*, Howard W. Sams, London, UK, 1985.

[16] T. H. Lee, *The Design of CMOS Radio-Frequency Integrated Circuits*, Cambridge University Press, Cambridge, UK, 2nd edition, 2004.

[17] Y. Sun and J. K. Fidler, "Design method for impedance matching networks," *IEE Proceedings - Circuits, Devices and Systems*, vol. 143, no. 4, pp. 186–194, 1996.

[18] Y. Sun and J. K. Fidler, "Component value ranges of tunable impedance matching networks in RF communications systems," in *Proceedings of 7th International Conference on HF Radio Systems and Techniques (Conf. Publ. No. 441)*, pp. 185–189, Nottingham, UK, July 1997.

[19] J. K. Fidler and Y. Sun, "Computer-aided determination of impedance matching domain," in *IEE 12th Saraga Colloquium on Digital and Analogue Filters and Filtering Systems*, pp. 1/1–1/6, London, UK, November 1992.

[20] M. Thompson and J. K. Fidler, "Determination of the impedance matching domain of impedance matching networks," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 51, no. 10, pp. 2098–2106, 2004.

[21] F. Ellinger, H. Jackel, and W. Bachtold, "Varactor-loaded transmission-line phase shifter at C-band using lumped elements," *IEEE Transactions on Microwave Theory and Techniques*, vol. 51, no. 4, pp. 1135–1140, 2003.

[22] F. Ellinger, R. Vogt, and W. Bachtold, "Ultra compact, low loss, varactor tuned phase shifter MMIC at C-band," *IEEE Microwave and Wireless Components Letters*, vol. 11, no. 3, pp. 104–105, 2001.

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