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Design and implementation of real time wideband channel simulator

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Abstract

This paper describes the design and implementation of a DSP based real time wideband channel simulator. The simulator implementation uses a floating point (TMS320C6713) and a fixed point (TMS320C6416) DSPs.The simulator has 8 taps and baseband bandwidth of 20 MHz. It has flexibility to generate several channel models under varied environmental conditions. To validate the functionality of the simulator, the baseband data is applied to the simulator input and its output is statistically analyzed and the results are compared with those predicted analytically.

Keywords: Baseband, Channel models, Fixed point, Floating point, Simulator

1 Introduction

Wireless communications are inherently unreliable due to their time varying nature, multipath propagations and presence of interference signals from other users. In the presence of these impairments, substantially higher power must be transmitted to overcome these impairments inorder to acheive acceptable symbol error rate in any kind of radio channel. To design reliable and efficient wireless systems, it is essential to understand the behavior of radio channels in different environments.

Statistical channel modeling plays a vital role in the design of reliable wireless communication system. Channel modeling is the first step towards the efficient wireless system design. The purpose of channel modeling is to compute and estimate the various first and higher order statistical parameters of the fading channel. These parameters include Doppler spread, the time constants of fading, average fade duration, level crossing rates, amplitude probability distribution functions and the coherence bandwidth. For this purpose, measurements have been taken in different environment to characterize the channel.

Over the past few decades, a number of experiments have been performed to characterize mobile channels in urban, suburban, mountainous, wooded and highway environments [1-16]. On the basis of these measurements, several channel models have been proposed to explain the observed statistical nature of the fading channels between fixed base stations and mobile stations. These include short term fading models like the well-known Rayleigh, Rice [17], Hoyt [18], Nakagami-m [19] and Weibull [20] and for longer term lognormal model has been used [6,21].

To evaluate the design and performance of a communication system, it is desirable to evaluate it in realistic situations. The experiments can be performed directly in a vehicle, driving through different environments. However, this is a time-consuming and expensive task and it requires the presence of measurement equipments with proper calibrations. Moreover, the field trials can be affected by unintended uncontrollable circumstances. The inexpensive and flexible option is to use a real time channel emulator and measure the performance in a laboratory environments as in [22-24]. The commercially available channel emulators available may not offer the user enough flexibility when configuring the wireless channel parameters to test the system under different environmental conditions. Such simulators do not cover V2V scenarios under different channel models like Hoyt, Rice Hoyt etc. A low cost channel simulator is therefore required that models different scenarios and at the same time provide the user flexibility to measure the performance of the wireless transceiver under environmental conditions.

Over the past few decades, efforts have resulted in several designs and implementation of real time simulators. Early efforts were based on analog components

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[25-28]. The development of real time simulator starts in 1973 when [25] developed the first Rayleigh based channel simulator. The simulator used Zener diode to generate Gaussian random variable. But with the advent of digital computers, micro-controllers, fast Analog to Digital Converters (ADCs) and Digital to Analog Converters (DACs), the analog components were replaced by digital thereby increasing the reliability and flexibility of simulators. Comroe et el [29] first used discrete digital logic in its simulator. With the development of High Speed Digital Signal Processors (DSPs), the DSP based simulators were developed. Goubran et al [30] used 16 bit fixed point DSP for implementation and simulated the Gaussian quadrature components along with the log-normally distributed Line of Sight (LOS) component. Turkmani et al [31] used TMS320 E15 DSP chip for the development of a narrow-band simulator. Cullen et al [32] reported a frequency selective simulator using TMS32050 DSP and IMSA110 integrated circuits. It had a baseband bandwidth of 10 MHz and maximum Doppler frequency of 100 Hz. Chen et al [33] used TMS320C31 DSP to design a frequency selective simulator. Salkintzis et al [34] developed 6 taps wide-band channel simulator having maximum signal bandwidth of 20 MHz. It used two 32 bit DSP floating point processors. Papenfuss et al [35] used a hybrid DSP FPGA architecture to build a wide-band channel simulator. It was capable of simulating 12 delay taps and had a baseband bandwidth of 5 MHz. Satellite Channel simulator has been developed in [36] using TMS320C6701 DSP platform. Kominakis et al [37] developed a narrow-band fast and accurate simulator. Khars et al [38] developed a 5 MHz 12 taps wide-band simulator using 12 DSPs (1 for each tap) for the generation of complex coefficients. A narrow-band DSP based channel simulator has also been developed in [39]. Over the last decade, the use of Field Programmable Gate Arrays (FPGAs) in DSP applications has become quite common. The FPGA based simulators have also been developed and their implementations have been described in [40-45].

One important application of wireless communication is Vehicle to Vehicle (V2V) communications where both the transmitter and receiver are in motion. The V2V communication finds its applications in mobile ad-hoc wireless networks, intelligent highway systems, emergency, military and security vehicles. The implementation of V2V communications enhances road safety due to reduction in the number of accidents, improvement in highway traffic flow efficiency and real time data sharing without involving the cellular network which leads to efficient fuel consumption and reduced travel time. The statistical model for vehicle to vehicle communication was first proposed by Akki and Haber [46] and its statistical properties reported in [47]. This model covers Rayleigh distribution only with both inphase and quadrature components having identical variances. Matolak et al [48] after performing measurements in five different cities, models the channel as Weibull fading channel. Based on the work of [47], many V2V simulators have been designed and implemented. Cox et al [49] presented a discrete line spectrum based approach to simulate the channel. The work in [50] was based on sum of sinusoids (SOS) approach for simulator design. The simulator proposed in [51] is based on Kullback-Leibler divergence which is compared with IFFT based approach of simulator design. Borries et al [52] used Gaussian quadrature rules for simulator design. Zaji et al [53] proposed an efficient sum of sinusoids (SOS) based approach for V2V simulator design. All the simulator design approaches mentioned above are restricted to V2V Rayleigh fading channel only.

The simulators mentioned above may be classified into three categories. The first category uses the sum of sinusoid (SoS) approach for generating the fading channel coefficients. This approach has the drawback of multiple *Sine* function calls which makes it computationally expensive to implement in real time. Secondly this kind of simulator does not produce the channel with the statistical properties that match with the theoretical values. Another class of simulators uses IFFT based approach to generate the required channel coefficients. This approach is computationally efficient. The drawback is that it works on a block of data and can not be used for the streaming data in real time. The approach used in this paper, is the Filter based approach. This is computationally efficient as well as produces channel coefficients having more accurate statistical properties.

The proposed simulator is a modified form of the simulator described in [37]. The proposed simulator uses a generalized Wideband Nakagami Hoyt with diffused line of sight channel model for Vehicle to Vehicle communication [54] environment to generate real time fading data. It covers Rayleigh, Rice, Rice-Hoyt, Lognormal and static channels as its special cases. The multipaths have been modeled as Tap Delay Line (TDL) filter. Efficient implementation of optimal TDL filter has been performed over the TMS320C6416 DSP processor. The novel simulator implementation uses two DSP (TMS320C6713 and TMS320C6416) boards along with one wide bandwidth (Microline ORS114) I/O daughter board. To the best of authors' knowledge, to date such real time simulator has not been proposed and implemented.

The remainder of this paper is organized as follows. Section 2 presents the brief overview of the proposed Diffused Nakagami-Hoyt V2V channel model. Section 3 describes the channel simulator design philosophy and architecture. Section 4 shows the outcome of the simulator and their comparison with the analytical expressions. Finally, Section 5 concludes the paper.

2 Brief channel model description

In V2V communications, the received signal consists of direct (LOS) and indirect (NLOS) component. The direct component may or may not be present depending on the presence or absence of obstacles between the transmitter and the receiver. The direct component may be further divided into a clear LOS between the receiver and the transmitter or a diffused LOS. The value of diffused LOS is negligible when the buildings are of steel or reinforced concrete but they must be considered for the wooden and bricks building. In rural areas, most of the building are made of wooden or bricks wall hence while modeling the channel, the diffused LOS component must be considered [55]. In V2V communications as mentioned by [56,57], when the antennas are inside the car, the shadowing must be considered due to the presence of roof top surface.

Youssef et al [16] established after taking the measurements in the rural environment that the channel is more accurately modeled only when the variances of Inphase and Quadrature components are different. The argument was further supported by [58] where the model matches the measured data for the cases of unequal variances. For V2V communication, [57] explained the case when the distance between the vehicles exceeds 70-100 m, the Nakagami m-factor is observed to be less than unity, which corresponds to the case of unequal variances of the Gaussian quadrature components. Further as found from the V2V measurements (antennas inside car) results in 5 GHz frequency band [48,59], the m value of each tap of the channel model described is found to be less than unity (0.75-0.89) which from [16] corresponds to the value of q (0.5-0.707).

Based on these, Akram et al [54] proposed Nakagami Hoyt V2V model with diffused line of sight under the assumption that omnidirectional antennas have been used. The proposed channel model $H(t)$ is a generalized model that covers the V2V environment as well.

$$H(t) = \rho(t) + \mu(t) \tag{1}$$

It considers, the lognormally distributed diffused LOS component $\rho(t) = Ae^{z(t)}$ and a NLOS component having Hoyt distributed amplitude envelop $\mu(t) = \mu_1(t) + j\mu_2(t)$ under the assumptions that both transmitter and receiver are in motion. $\mu_1(t)$, $\mu_2(t)$ and $z(t)$ are the real Gaussian random processes with zero mean and variances σ_1^2, σ_2^2 and σ_3^2 respectively and A is the direct LOS component. $q = \frac{\sigma_1}{\sigma_2}$ and V_2 and V_1 are the velocities of transmitter and receiver respectively and $a = \frac{V_2}{V_1}$.

The time autocorrelation function of the random process $H(t)$ is derived in [54]

$$\begin{aligned} R_H(\Delta t) &= A^2 \exp[\,\sigma_3^2(1 + J_0(2\pi f_{m3}\Delta t))] \\ &+ \frac{1+q^2}{2q^2}\sigma_1^2 J_0(KV_2\Delta t)J_0(KV_1\Delta t) \end{aligned} \tag{2}$$

where, $J_0(.)$ is the zero-order Bessel function. $q = \frac{\sigma_1}{\sigma_2}$, V_2 and V_1 are the velocities of transmitter and receiver respectively, $K = \frac{2\pi}{\lambda}$ and f_{m3} is the LOS component maximum Doppler.

The power spectral density of the proposed model is found as [54],

$$\begin{aligned} S_H(f) &= \int_{-\infty}^{\infty} R_H(\Delta t)e^{-j2\pi f\Delta t}d\Delta t \\ &= S_\rho(f) + S_\mu(f) \end{aligned} \tag{3}$$

where,

$$S_\rho(f) = A^2 e^{\sigma_3^2}\left[\delta(f) + \sigma_3^2 f_{m3}\frac{rect(\pi f/f_{m3})}{\sqrt{f_{m3}^2 - 4\pi^2 f^2}}\right] \tag{4}$$

for $\sigma_3 < 0.3$ and,

$$\begin{aligned} rect(t/T) &= 1, t \le |T| \\ &= 0, otherwise \end{aligned}$$

$$\begin{aligned} S_\mu(f) &= \frac{1+q^2}{2q^2\pi^2 f_{m1}\sqrt{a}}\sigma_1^2 \\ &\times K\left[\frac{(1+a)}{2\sqrt{a}}\sqrt{1-\left(\frac{f}{(1+a)f_{m1}}\right)^2}\right] \end{aligned} \tag{5}$$

where $K(.)$ is the elliptical integral function of first kind, $a = \frac{V_2}{V_1}$, f_{m1} , f_{m2} are the maximum Doppler shifts due to the motion of the receiver and transmitter respectively with $f_{mi} = \frac{V_i}{\lambda}$. Therefore, $f_{m2} = af_{m1}$.

3 Simulator description

3.1 Design philosophy

In efficient real time systems design all the available system resources are efficiently utilized in order to minimize the cost and maximize the productivity. For the data acquisitioning at high data rate, the DSPs can not be interfaced directly with high speed ADCs and DACs

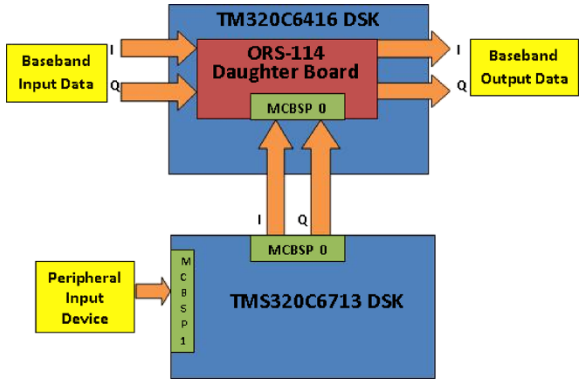

Figure 1 Channel simulator block diagram.

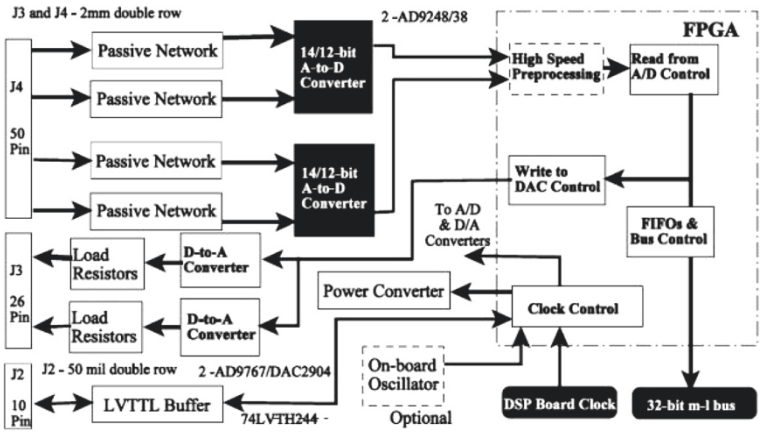

Figure 2 ORS-114 block diagram.

because of its I/O bandwidth limitations. The best solution is to use FPGA for this purpose. Therefore, Microline ORS114 daughter board was used for this purpose. The board consists of a vertex-2 FPGA, multiple channel ADC and DAC, FIFO memory and control circuitry used to synchronize the data input output events with DSP. The board is mounted over the peripheral expansion of TMS320C6416 fixed point DSP Starter Kit (DSK) which performs the TDL filtering. Since filtering operation needs to be performed at high data rate, for this purpose an optimal TDL filter need to be implemented. This can be done over fixed point processor of high clock rate. Hence for that purpose TMS320C6416 processor with 1 GHz clock have been selected. The channel coefficient generation depends upon the time variations of the scatterers surrounding the transmitter and receiver. These variations are normally much slower as compared to the baseband data rate. Therefore for the channel generation purpose a processor with lower clock rate is adequate and a TMS320C6713 32 bit floating point processor is employed. The purpose of floating point processor is to generate the channel coefficients accurately with high precisions.

3.2 Simulator design specification

Figure 1 shows the overall block diagram of the channel simulator. It consists of two DSKs communicating with each other using Multiple Channel Buffered Serial Port 0 (MCBSP0). The TMS320C6713 DSK board acts as a Master device. It generates and transmits channel

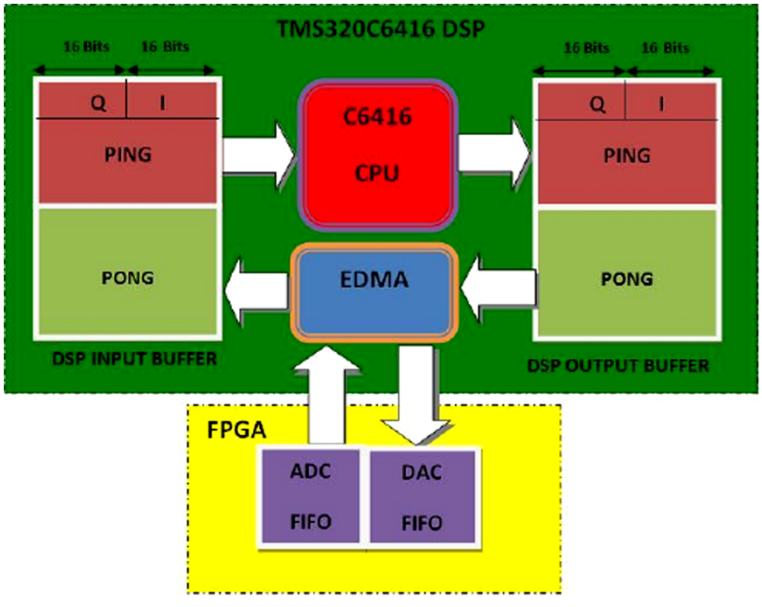

Figure 3 Block diagram showing input output operations.

Table 1 Timing diagram

Time Line ⟶	0	NT_s	$2NT_s$	$3NT_s$
EDMA Transfer	ADC⟶PING IN	PONG OUT⟶DAC	ADC⟶PONG IN	PING OUT⟶DAC
DSP Processes	IDLE	PING BUFF	IDLE	PONG BUFF

coefficients to the primary TMS320C6416 DSK board which acts as a slave. The system runs according to the following specification:

- TMS320C6416T DSK board having 1 GHz fixed point processor works as a primary board to accept the baseband input and generate output;
- TMS320C6713 DSK board having 225 MHz floating point processor works as a secondary board that will generate channel taps at the required rate;
- Input Baseband data bandwidth 20 MHz (10 MHz each I & Q);
- Maximum number of Taps (channel coefficients) generated N = 8;
- Maximum Doppler frequency that can be set = 480 Hz;
- ADC and DAC Buffer size = 1024 Elements (16I + 16Q)= 32 bits;
- ADC and DAC resolution = 14 bits;
- Maximum sampling rate of ADC and DAC = 25 MHz;
- Transfer rate of channel coefficients = 16 kHz (2 kHz per tap);
- Maximum excess delay = 1024 samples which on 25 MHz sampling frequency becomes 41 μ sec.

3.3 Simulator functionality

The simulator performs the following tasks.

3.3.1 Baseband data acquisition

The baseband data acquisition uses Signalware's ORS-114 daughter board. This card is designed to facilitate rapid construction of prototypes or small to medium production runs with minimum time-to-market. This peripheral card provides flexible analog input and output for applications with a Texas Instruments (TI) Digital Signal Processors (DSP). It mounts on a card that contains TI TMS320C6xxx DSPs made by ORSYS, Inc. These DSP cards, known as the "micro-line" series, contain the processor, DRAM memory and an expansion interface which allows the peripheral card full access to all of the DSP's resources. The hardware block diagram of ORS114 board is shown in Figure 2.

The daughter board is configured to use 2 channels ADC and DAC working at 25 MSPS each and transferring 14 bit data in and out of DSP. The data transfer is done using Enhanced Direct memory Access (EDMA) interface configured with optimal External memory Interface (EMIF) setting to read and write data. The pin configuration detail is given in [60].

Ping Pong buffering technique described in TI documentations at [61] has been used to perform data transfer efficiently between the I/O devices and Internal Memory (SRAM) of DSP. EDMA engine performs the data transfer between the ping/pong buffers and I/O device alternately and a pingpong flag ensures that the DSP is processing the buffer that is not being overwritten by the EDMA. Since EDMA runs independently from the CPU, the CPU can continue to process the block of data that is in the ping buffer while the EDMA is writing data on the pong buffers and vice versa. In order to remain synchronous with EDMA and void the data loss, it is essential for CPU to finish the processing before the next EDMA interrupt is generated. This Hardware interrupt is generated every time the EDMA completes data transfer.

After reset, the DSP performs all the necessary initializations. It configures EMIF settings, initializes the Daughter board, configures EDMA channels to start data transfer and waits for the peripheral device to input the channel parameters. For the ADC Sampling time T_s and PING/PONG buffer size N, the data transfer flow is shown in Figure 3. The timing diagram is shown in Table 1.

3.3.2 Primary secondary board interface

The function of the primary secondary board interface is to obtain the channel coefficients in real time. For this purpose the Multiple Channel Buffered Serial Port (MCBSP 0) present on the external peripheral interface of the TMS320C6416 DSK board, has been used. The port is directly connected with the MCBSP 0 of the secondary board in Master/Slave configuration such that the secondary board that is generating channel coefficients work

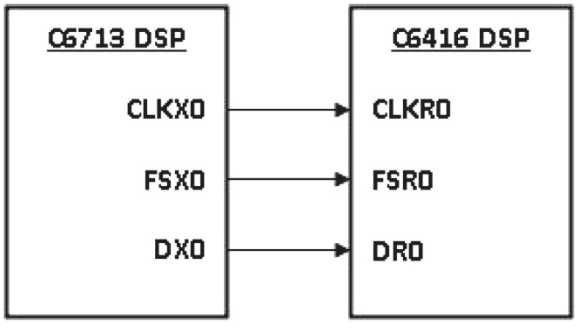

Figure 4 MCBSP connection between the two DSPs.

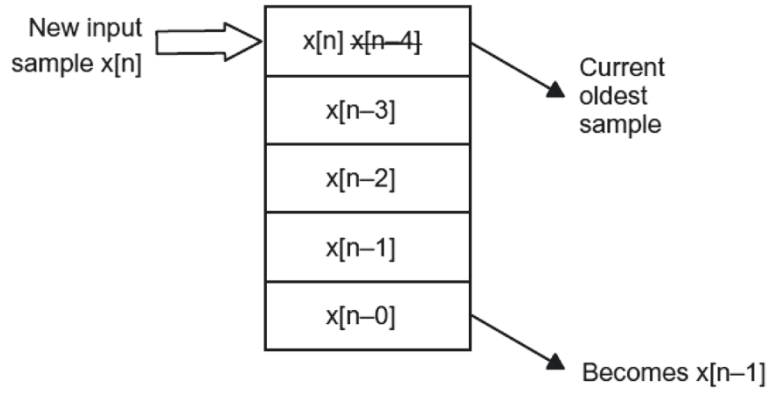

Figure 5 Pointer manipulation using circular addressing.

as Master device as it also generates clock and frame signal for the serial port whereas the primary board acts as a Slave and use these signals to get data. The block diagram of the connection between the two DSPs via MCBSP ports have been shown in the Figure 4.

After connecting the two DSPs together the next step is to configure the ports so that the data can be transmitted and received successfully. The ports are configured by the setting the appropriate values of the four serial port registers. They are Receive Control Register (RCR), Transmit Control Register (XCR), Sample Rate Generator Register (SRGR), Pin Control Register (PCR).

The details of how to set these registers are given in TI documentation [62]. The values are set so that one frame consisting of 8 channel coefficients (each of 32 bits) is transmitted in 500 μ sec that results in a transmission rate of 16 kHz per coefficient.

Again, EDMA along with ping pong buffering technique is used to perform this transfer efficiently. At the transmitting end, the EDMA interrupt is generated periodically and at the same time, the CPU generates new channel coefficients. Whereas, at the receiving end, when a complete frame is received an interrupt is generated and the channel coefficients are updated.

3.3.3 Tap delay line filtering

Tapped Delay Line Filter is the basic block of many digital signal processing applications. It is based on the following equation

$$y[n] = \sum_{k=0}^{M} x[n-k].h[k] \tag{6}$$

where $y[n]$, $x[n]$, $h[n]$ are samples of the output, input and filter coefficient respectively at *nth* sample instant of a digital system of order M.

As seen from (6), in order to obtain an output $y[n]$ in real time, a buffer of M previous values (delay line) need to be maintained along with the current sample. Typically, a pointer is set up at the beginning of the sample array (oldest sample) and then manipulated to access the consecutive values.

Whenever a new sample needs to be added to the delay line all the values need to be shifted down. For large values of M (delay line), this will cause additional overhead of shifting the large amount of data. The alternate approach is to overwrite the oldest value. This can be implemented by using circular mode for pointer access.

The input data buffer has finite size and has to be accessed circularly as the new samples are continuously written into the buffer the previously stored (oldest samples) need to be overwritten so that the buffer memory is reused. When the pointer reaches the last location of the buffer, it needs to wrap back to the beginning of the buffer. This would normally involve some amount of software overhead. When Input buffer addressing is defined as circular, the pointer automatically wraps back to the top whenever the bottom of the buffer is reached. Figure 5 illustrates the circular addressing. The input buffer is made circular for that purpose it must be properly aligned in the internal memory. The detail of how to set the buffer as Circular is given in [63].

TDL Filter can be implemented in several ways depending upon the application. Here, the filter is modeled as a frequency selective channel, where the channel taps are

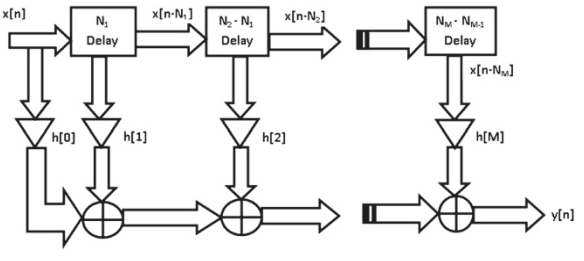

Figure 6 Tap delay line filter model.

Table 2 Four taps TDL resources allocation for main loop

FU Cy	1	2	3	4	5	6	7	8
.M1	MPY I4	MPYH I1	MPY I1	MPYH I2	MPY I2	MPYH I3	MPY I3	MPYH I4
.M2	MPYHL Q4	MPYLH Q1	MPYHL Q1	MPYLH Q2	MPYHL Q2	MPYLH Q3	MPYHL Q3	MPYLH Q4
.L1	SUB I3	ADD I3	SUB I4	ADD I4	SUB I1	ADD I1	SUB I2	ADD I2
.L2	ADD Q3	ADD Q3	ADD Q4	ADD Q4	ADD Q1	ADD Q1	ADD Q2	ADD Q2
.S1		ADD	B	ZERO	SHR		ADD	
.S2				ZERO	SHR			ADD
.D1	LDW	LDW			LDW	LDW	STH	
.D2					SUB			STH

assumed as multipath fingers located at multiple of sampling time T_s . The $N = M + 1$ tap time intervals are assumed as τ_i where i varies from 0 to M and $\tau_0 = 0$. The channel model is shown in Figure 6. The tap index N_i is related with τ_i as

$$N_i = \left\lfloor \frac{\tau_i}{T_s} + 0.5 \right\rfloor \tag{7}$$

where $\lfloor . \rfloor$ indicates the truncation operation. For the buffer size L, the maximum excess delay that last finger can be computed as

$$\tau_{max} = LT_s \tag{8}$$

Using the pipelining approach mentioned in [64] the code has been optimized for $N = 8$ taps. The inner loop was completely unrolled to reduce the loop overhead, the dependency graph was created and the instructions were pipelined to reduce the number of cycles. The optimized code consists of 3 parts. The *prolog*, the *mainloop* and *epilog*.

The prolog consists of initialization of local variables, pushing registers over stack for usage inside the function, loading taps coefficients $h[n]$ from memory into registers and defining input buffer as circular. Defining the input as circular buffer removes the overhead of an additional branch instruction inside the loop. The use of circular buffer prevents the constant test of wrapping. The prolog is to be executed once for L size input buffer. It takes 45 cycles to execute this code.

The main loop is also known as kernel of the program which is executed most of the time. It is optimized and instructions are scheduled to maximize the utilization of the CPU resources. For N taps it is executed $2N$ times per input sample. For 4 taps, the resources allocations are shown in Table 2. It is also shown that loading of data from memory and its storage into memory are done at the same time using .D1 and .D2 functional units. whereas branching instruction, re-initialization, output storing and counter increments have also been scheduled. *STH* instructions have been used to store the sample output back into the internal memory, *ZERO* to re-initialize the output registers back to zero for the computation of

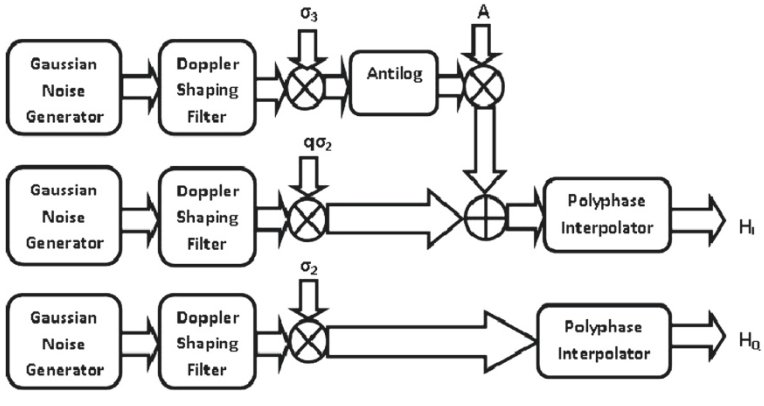

Figure 7 Single tap generation using filter method.

Table 3 Various channel models for simulation

	$A = 0$	$A \neq 0$	
		$z(t) = 0$	$z(t) \Rightarrow$ *Gaussian*
$q = 1$	Rayleigh	Rice	Log-Normal Rice
$0 < q < 1$	Hoyt	Rice Hoyt	Diffused Hoyt
$\sigma_2 = 0$	-	Static	Lognormal

next sample output and *SHR* to bring the output in the required Q3.13 format.

The epilog consists of the remaining part of the function. This include remaining loop portion, popping data back to the registers and branch out of the function. This part takes 42 cycles to execute.

3.3.4 Channel gains generations

The channel coefficients have been generated using a floating point TMS320C6713 DSP. Kominakis et al [37] describes the efficient method of generating the channel gains. It uses Infinite Impulse Response (IIR) Doppler filter along with the polyphase interpolator for the generation of correlated Gaussian channel coefficients. The original approach was for flat fading Rayleigh channel only. It was modified for the more generalized 8 taps frequency selective Nakagami-q (Hoyt) mobile to mobile fading channel with diffused LOS.

The block diagram of the channel coefficient generation unit of the single (first) tap is shown in Figure 7. The block diagram represents a generalized channel model. By varying the values of parameters (a, q, σ_2 and A) different channel models can be obtained and simulated. These models are shown in the Table 3. For $a = 0$, the models are obtained for Base to mobile communication whereas $a > 0$ represents V2V communications.

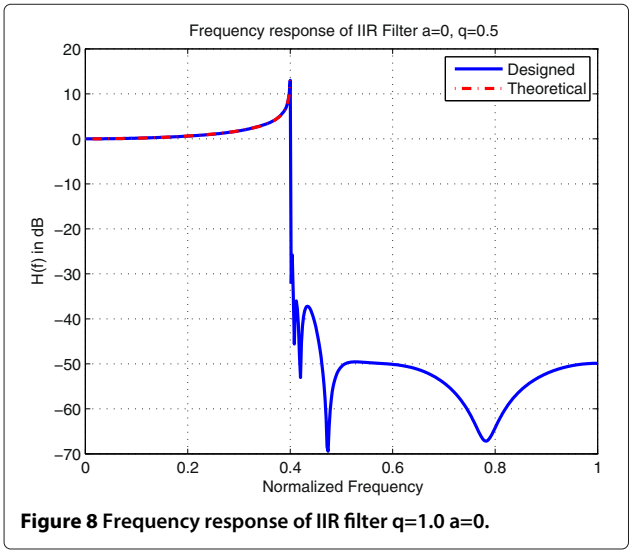

Figure 8 Frequency response of IIR filter q=1.0 a=0.

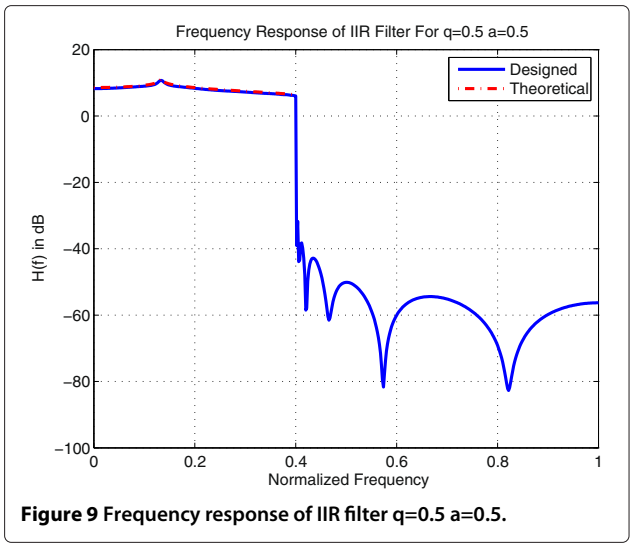

Figure 9 Frequency response of IIR filter q=0.5 a=0.5.

The Doppler Shaping Filter is implemented as an IIR Filter having the frequency response $\sqrt{S(f)}$ obtained by taking the Square root of (5). The filter has been designed for the Doppler rate of $f_d T_s = 0.2$. The higher rate is achieved by interpolating the channel coefficients I times using polyphase interpolator. For the Fade Rate ($f_d T_s$) of 0.01, the value of $I = 20$ is taken. For the maximum Doppler frequency of 160 Hz the channel sampling rate is set to 16 kHz.

The maximum Doppler frequency is configurable and is set using LCD Keypad interfacing of TMS320C6713 DSK (MCBSP1 port). This can go up to 480 Hz. For a single emulator run, it will remain unchanged. The filter coefficients are computed on the base of normalized Doppler frequency. The algorithm for filter coefficient generation uses fade rate ($f_d T_s$) of 0.01. For 160Hz Doppler the Sampling frequency (Filter coefficient update rate is 16 KHz).

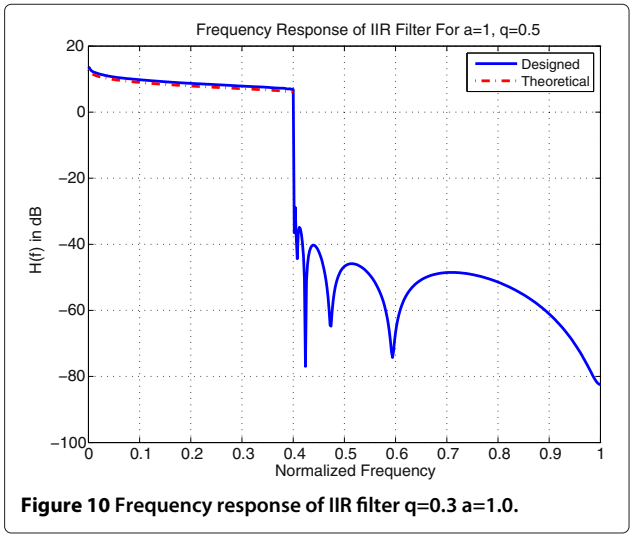

Figure 10 Frequency response of IIR filter q=0.3 a=1.0.

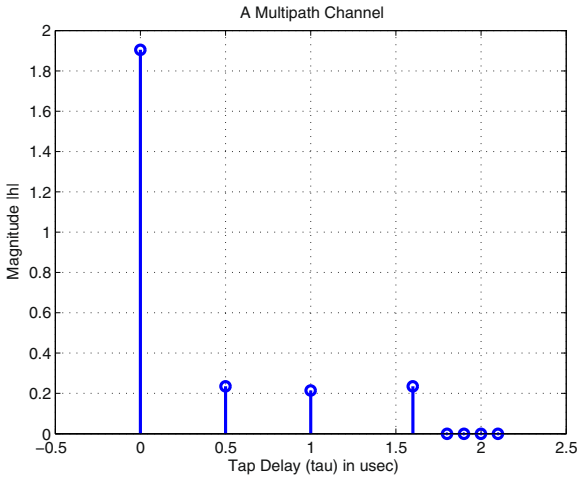

Figure 11 Channel magnitude impulse response.

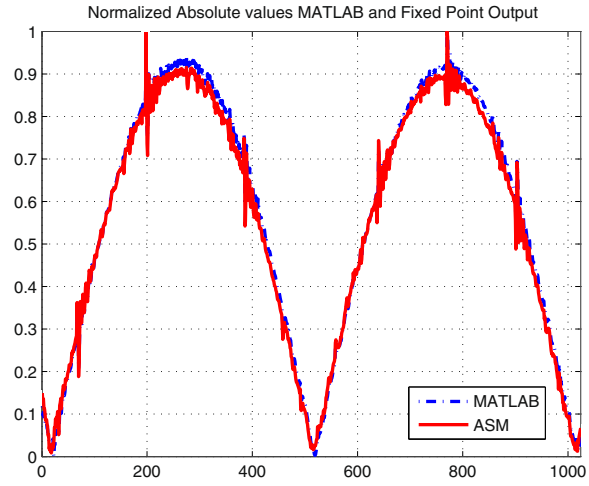

Figure 13 TDL filter output magnitude plot.

This means if the Doppler frequency is increased the sampling frequency will also be increased in the same proportion so as to make the fade rate constant. The increase in sampling frequency means MCBSP0 port data rate will be increased. This rate is software configurable and can be set by changing the value of Sample Rate Generator Register (SRGR) of the MCBSP0 port. The upper limit depends upon the complexity of the Channel coefficient generation algorithm and number of taps. For 8 taps, it is 480 Hz and this can be increased if we further optimize the channel generation code using some optimization techniques (reducing mathematical complexity and efficient use of DSP resources).

The interpolator is implemented as a polyphase filter with a windowed *sinc*(.) function impulse response. The algorithm for channel coefficient generation is modified in order to consider the generalized cases. Figures 8, 9, 10 show the frequency response of the modified PSD under different values of $a = (0, 0.5, 1)$, $q = (1.0, 0.5, 0.3)$, $A = 0$ and $\sigma_2 > 0$.

4 Results and comparison

A TDL filter with N taps is modeled here as a frequency selective multipath channel. Each tap is complex having defined location. The channel is assumed static for one buffer period of time. Both C and assembly functions were executed for $L = 1024$ I/O buffer size, data sampling frequency $Fs = 12.5MHz$ and $N = 8$ taps filter coefficients having values h={1.8362 - 0.5073i, -0.2169 + 0.0915i, -0.1448 + 0.1585i, -0.2169 + 0.0915i, 0.0, 0.0, 0.0, 0.0 } with corresponding tap locations at {0, 0.5, 1, 1.6, 1.8, 1.9, 2.0, 2.1} usec. The magnitude response $|h|$ of the channel is shown in Figure 11.

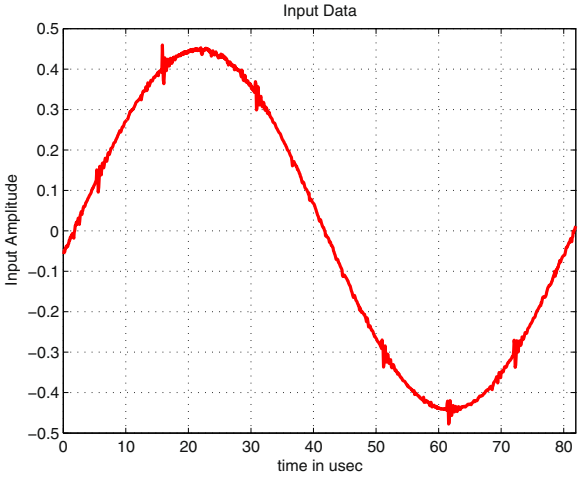

Figure 12 Input data on both I and Q channel.

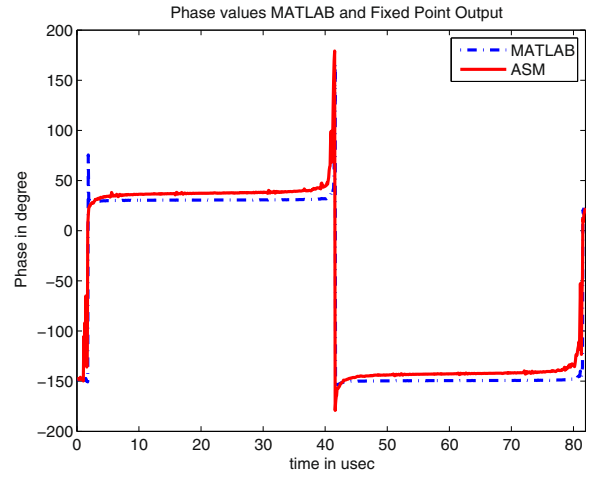

Figure 14 TDL filter output phase plot.

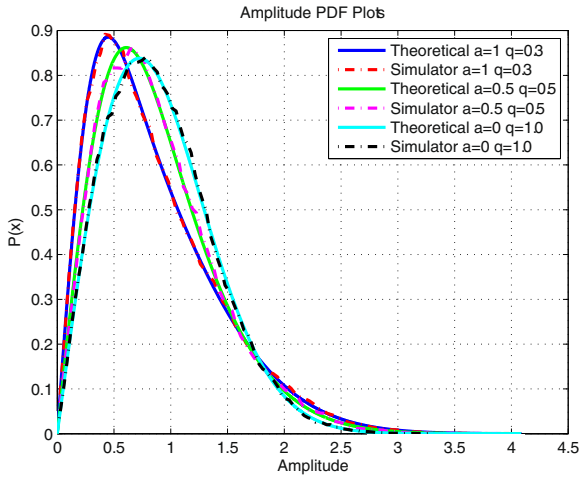

Figure 15 PDF plot for amplitude.

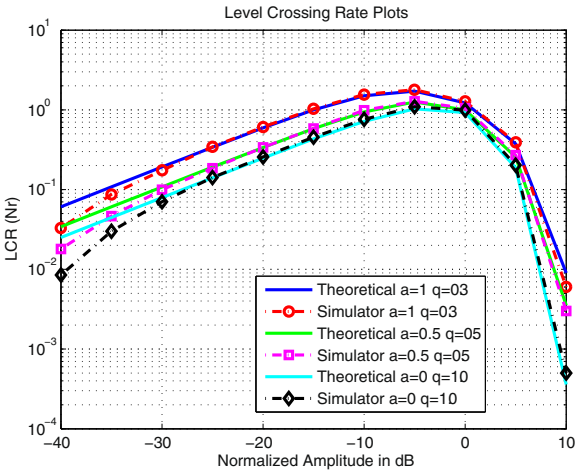

Figure 17 PDF plot for LCR.

Most V2V systems operate in frequency range 5-5.9 GHz [57]. Bwang et el [65] and Matolak et el [66] used 5.15 and 5.2 GHz carrier frequencies to simulate the V2V channel. Hence, the simulation was run with the following parameters, carrier frequency $f_c = 5.8GHz$, velocity of receiver $V_1 = 30km/hr$ which means $f_{m1} = 160Hz$, LOS component $A = 0$ for Hoyt model, three different values of $q = 1, 0.5, 0.3$ and three different values of $a = 0, 0.5, 1$.

The sinusoidal input shown in Figure 12 is applied on both I & Q channels. The output of both were found exactly match with each other. For fixed point C code, it takes 1460 cycles per sample to generate output whereas the optimized code gives output in 16 cycles per sample. From (8), the maximum excess delay τ_{max} the system can have is found to be 81.92 usec.

A comparison has been made for a given complex input between the outputs of the MATLAB complex FIR filter code with the fixed point assembly code and are shown in Figure 13 (Magnitude plot) and Figure 14 (Phase plot). The number of taps assumed are $N = 8$ with buffer size $L = 1024$. For C6416 DSP operating at $1GHz$, the cycle time becomes $1ns$ hence proposed algorithm will take around $16ns$ per sample which means that data with around $60MHz$ sampling frequency can be processed.

In order to verify the channel coefficient generation, the performance analysis of the Channel has also been

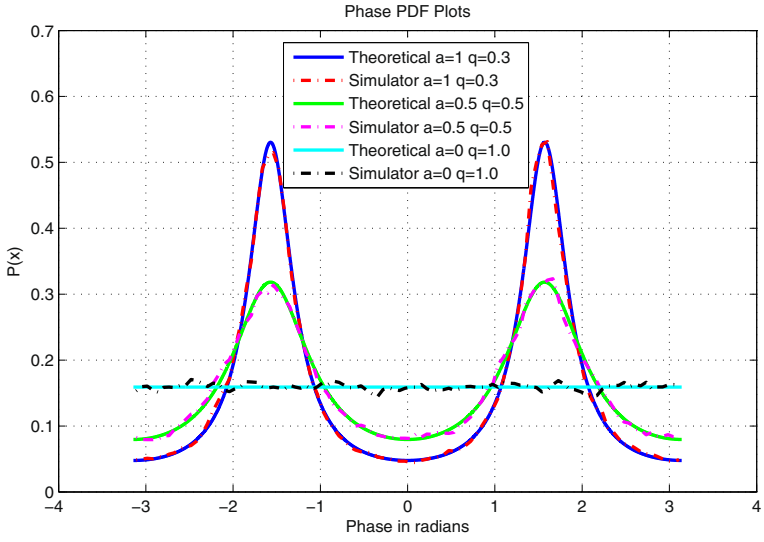

Figure 16 PDF plot for phase.

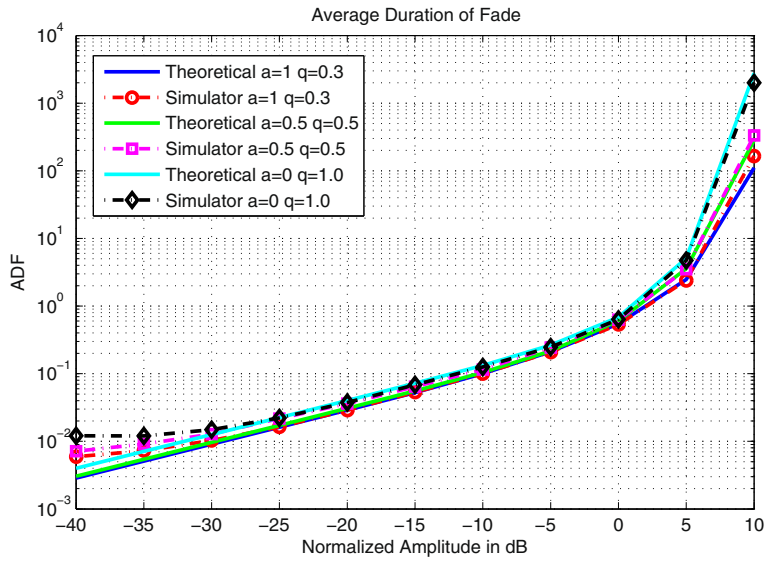

Figure 18 PDF plot for ADF.

done. The BPSK modulated data is applied at the input of the single tap channel and the output and Channel coefficients (400k samples) are stored in the *SDRAM* of TMS320C6416 DSP Board in real time. Since performance analysis is independent of data rate and sampling frequency, hence due to the limited size of *SDRAM* the sampling rate was set to 2 MHz and the input data rate to 200 kbps. The amplitude and phase Probability Density Function (PDF), Level Crossing rate (LCR), Average Duration of Fade (ADF) and Bit Error Rate (BER) plots are shown in the Figure 15, 16, 17, 18, 19 respectively. The plots are found to be closely matched with the corresponding theoretical plots. Mean square error (MSE) between the theoretical and simulated values of the amplitude, phase PDF, BER curves and LCR are shown in Table 4.

The proposed simulator is also compared with the one described in [67]. There is a significant difference between

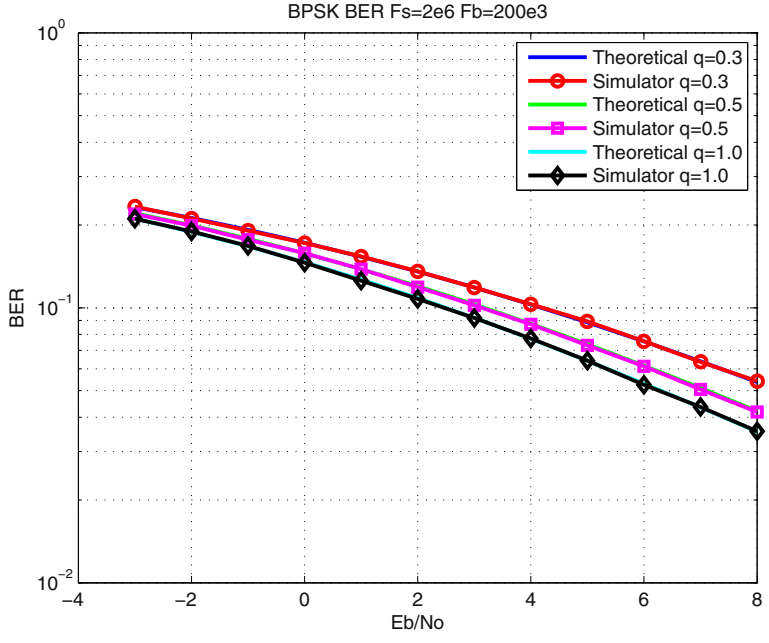

Figure 19 BER plot, BPSK modulation q=1, q=0.5, q=0.3.

Table 4 MSE of various quantities for a = 0.5

q	Envelope PDF	Phase PDF	BPSK BER	LCR
0.3	4.240×10^{-5}	4.647×10^{-5}	1.456×10^{-7}	13×10^{-4}
0.5	8.148×10^{-5}	3.371×10^{-5}	4.439×10^{-7}	6×10^{-4}
1.0	6.511×10^{-5}	2.586×10^{-5}	0.775×10^{-7}	11×10^{-4}

the philosophies of the two simulators. The simulator described in [67] requiring measured impulse response, generates channel coefficients from the measured channel transfer function. These channel coefficients operate on the information data to deliver performance in terms of error rate. This simulator essentially requires in field measurements. The proposed simulator does not require measured in-field data but uses the statistical models available in published standards, thus saving significantly on the cost of expensive field trials. The proposed simulator operates on the statistical parameters to generate real time channel coefficients, which then operate on the information data to generate performance in terms of error rates. The developed simulator can be used to operate on the in-field channel data provided we augment this simulator with a facility to convert the stored channel data into channel coefficients or channel statistics. It should be borne in mind that our interest has been to replace field environment by laboratory environment and by various options on choices of channel character.

5 Conclusion

In this paper, design and implementation of an efficient real time wideband simulator has been discussed. The simulator was run in real time with a known input and the output data was analyzed. The TDL filter has been optimally implemented over TMS320C6416 DSP. The output of the filter has been verified by comparing the simulator output with MATLAB. The pipelined architecture of the processor and the circular buffer have been efficiently utilized. The channel coefficients have been generated and analyzed. The BPSK modulated data has been input and the output has been stored. The bit error rate has been measured and compared with the theoretical data to verify the validity of the channel simulator.

Competing interests
The authors declare that they have no competing interests.

Authors' contributions
DSP based wideband real time simulator has been developed that is based on Nakagami Hoyt V2V channel model and is flexible to simulate the other channel models by just changing the parameters. Both authors read and approved the final manuscript.

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