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Intensity feedback-based beam wandering mitigation in free-space optical communication using neural control technique

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Abstract

Over the last two decades, free-space optical communication (FSOC) has become more and more interesting as an adjacent and/or alternative to radio frequency (RF) and optical fiber communications. The optical wave propagation in the FSOC channel is severely affected by atmospheric parameters, and it leads to the degradation of the data transmission quality and reliability. Among the various atmospheric effects, the beam wandering is the main cause of major power loss and cannot be solved without the incorporation of the beam centroid stabilization system. Therefore, designing a suitable opto-electronic assembly with a beam wandering mitigation system becomes significant to improve the performance of the FSOC system. A FSOC experimental setup is developed for the link range of 0.5 km in the college campus. A neural controller is designed for beam wandering mitigation. The neural controller processed the beam pointing (beam location) information obtained from an opto-electronic position detector (OPD) and then generated the necessary control outputs to the fast steering mirror (FSM) to steer the beam in the counter-direction to mitigate the beam wander at the receiver station. New design approach and architecture development for the implementation of the designed neural controller in the field-programmable gate array (FPGA) to mitigate the beam wandering are presented. The investigations on the performance of the neural controller in aiming a laser beam to be at a particular point on the detector plane are tested under dynamic disturbances generated at the transmitter in addition to the atmospheric effects through which the maximum correction capability of the developed neural controller is examined. Evidence of the suitability and the effectiveness of the proposed neural controller is evaluated in terms of beam centroid displacement, power spectral density (PSD), radial displacement on a 2D plane, effective scintillation index (ESI), Q-factor, and bit error rate (BER). The beam wandering range of -0.13 to +0.16 mm, maximum of 55 dB disturbance band attenuation with a frequency range of 0 Hz through 2 kHz, ESI of 0 to 0.15, Q-factor of 6, and BER of 6.45×10^{-9} are achieved due to the incorporation of the developed neural controller in different real-world environmental conditions.

Keywords: Non-linearity; Intensity feedback; Neural controller; Beam wandering; Scintillation and bit error rate

1 Introduction

Recent and rapid progress in information and communication technology has exceeded our expectations for meeting the requirements of multimedia society in the twenty-first century. Free-space optical communication (FSOC) is considered to be one of the key technologies for realizing very high speed multigigabit per second (multi-Gb/s) large-capacity terrestrial and aerospace communications [1,2].

The FSOC system provides a line of sight (LoS), wireless and high-bandwidth communication between remote sites. The FSOC system offers many transmission advantages including freedom from electromagnetic interference (EMI) and license or tariffs, flexibility, ease in installment, no need to dig up roads, last-mile access, service acceleration, metro network extensions, enterprise connectivity, fiber backup, backhaul, and high security [3,4]. In addition, a photonics-based approach is expected to bring such ultra-high data rate wireless technologies to potential users and to meet and explore real-world applications at the earliest opportunity as a technology driver [5]. However,

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the propagating optical wave is influenced in the FSOC channel by random atmospheric changes (wind speed, temperature, relative humidity, and pressure) [6], thermal expansion, weak earthquakes, and typical high-rise building sways which result in decreasing the average received power, increasing the bit error rate (BER), and severely degrading the communication link quality/reliability [7-9]. These are all the general problems that require attenuation to be dealt with. The major effects due to the random fluctuations of the atmospheric turbulence are (i) optical scattering and observation (characterized by atmospheric attenuation); (ii) random optical power fluctuation (characterized by scintillation index); (iii) beam wandering, i.e., beam surface global (temporal) tilt due to beam centroid displacement on the detector plane (characterized by effective scintillation index); and (iv) wavefront distortions, i.e., beam surface (spatial) local tilt (characterized by the Zernike polynomials) [10-12]. The conventional data coding and/or modulation techniques can be used to equalize/compromise the first two effects with respect to weather conditions at a given instant of time [13,14]. The third and fourth effects cannot be compromised without incorporating the adaptive optics elements [15,16]. During data transmission, the angle between the transmitter-receiver LoS and the transmitting beam axis must be kept within a fraction of the transmitting beamwidth which may be as small as a few microradians. The increase in the transmitting beam divergence angle/diameter is one way to maintain the link between the transmitter and receiver. It is clear that an overly wider beam will increase the required laser power, which increases the terminal cost and complexity. On the other hand, an overly narrow beam may result in a cutoff of the communication when there is building sway and/or beam wandering [2,3,7,8]. The existence of a perfect LoS and continuous beam alignment between the communicating optical antennas is one of the key requirements for a successful installation of an FSOC system. To ensure an uninterrupted data flow, auto-alignment transmitter and receiver modules are necessary [12,17,18]. The data loss due to weak scintillation effects can be recovered using various data coding techniques developed for wire- and fiber-based communication systems [13,14]. In contest, beam wandering and deep signal fading (wavefront distortions) represent unique and significantly more challenging problems, which cannot be resolved using conventional data coding techniques, and a major incentive for the incorporation of adaptive optics technology (beam wandering mitigation and wavefront corrections) into the FSOC architecture is an active prevention of long-term data loss [12,15,16]. The first and most important requirement for the successful installation of FSOC is beam steering (reduction of focal spot wander) that mitigates the beam wandering (temporal distortions) [1,16-18] which

is the research component and main contribution in this work.

Therefore, designing a suitable control system for beam auto-aligning, tracking, and positioning (ATP) to mitigate the beam wandering so as to significantly improve the beam stability on the receiver plane becomes significant. The complexities of a beam ATP controller design for the beam wandering mitigation process is increased due to inherent non-linearity and hysteresis of opto-electronic components involved in the beam steering process, thereby making the control of a non-linear system non-trivial [19-21]. The Artificial Neural Network (ANN) is the most popular intelligent tool especially for non-linear function approximation and control applications due to its high ability of learning from sample data and yielding better results to the new data [20-22]. A new design approach is introduced in this paper for the hardware implementation of a neural controller in a field-programmable gate array (FPGA) to operate the beam ATP process at a faster rate and also in parallel. The unipolar non-return to zero on-off keying-intensity modulation-direct detection (UNRZ-OOK-IM-DD) scheme is used for data transmission [23,24]. In order to intensively evaluate the performance improvement of FSOC due to the beam ATP control system, the time series plot of beam centroid displacement (wandering) on a 2D optoelectronic position detector (OPD) plane received signal power fluctuation and the demodulated data are continuously recorded and used to carry out on/off line analysis and compute various communication parameters. The effective scintillation index (ESI), i.e., scintillation due to beam wandering, is estimated by [4,11].

$$ESI = (\langle I^2 \rangle / \langle I \rangle^2) - 1 \tag{1}$$

where I is the received irradiance and $< ^{\cdots} >$ is the temporal mean (ensemble average) intensity of the optical beam at the receiver which is equal to a long time average assuming the process to be ergodic and a photodiode is a single point detector. The received data are continuously recorded in the real-time oscilloscope, and the data statistics are used to evaluate the link performance by estimating the signal to noise ratio (SNR) that includes the received signal power and system noise as [10,24]

$$SNR = \left(P_{top}^2 - P_{base}^2\right) / \left(\sum \sigma_{top}^2 + \sum \sigma_{base}^2\right)$$
 (2)

where $P_{\rm top}$ and $P_{\rm base}$ are the means of most predominant peaks of a histogram constructed for high ('1') and low ('0') logic levels, respectively, and $\sigma_{\rm top}$ and $\sigma_{\rm base}$ are the standard deviations for the means of high ('1') and low

('0') logic levels, respectively. The system metric Q-factor (linear) is calculated by [24]

$$Q = (P_{\text{top}} - P_{\text{base}}) / (\sigma_{\text{top}} + \sigma_{\text{base}})$$
 (3)

The theoretical BER is estimated using Equation 3 and complementary error function (erfc) as [10,24]

$$BER = 0.5erfc(Q/\sqrt{2})$$
 (4)

Equations 1, 2, 3, and 4 are used to quantitatively analyze the FSOC data link performance improvements so as to understand and ensure the greatest contributions of the developed new ATP control system.

The rest of the paper is organized as follows: 'Section 2' presents the backgrounds and related works, 'Section 3' describes the experimental setup construction and beam spot position data processing, 'Section 4' explains about the novel digital architecture designed to implement the neural controller and universal asynchronous receiver transmitter (UART) manager, 'Section 5' discusses the experimental results and data analysis, and 'Section 6' draws some conclusions.

2 Background and related works

In the last few years, a lot of controller designs related to laser beam ATP have been remarkably carried out and can be found in literature. The publications/results closely related to our work are briefed in this section. Two optimization models are developed and simulated by Xian Liu for continuously adjusting the transmitter power, wavelength, telescope gain to mitigate the beam LoS deviations due to building sway, and atmospheric interference. The continuous adaptation of these parameters is difficult in real-time implementation, and also, this approach increases terminal cost and complexity [3]. E. Ciaramella et al. have presented a dedicated electronic control unit that effectively tracks the signal beam wandering caused by atmospheric turbulence and mechanical vibrations in a wireless optical data link of 212 m between two buildings in Pisa, Italy. The tracking beam is coupled with the single-mode fiber (SMF). In this work, two separate optical beams, one for data transmission and another for beam steering control (beacon beam), are used [4]. Hanling Wu et al. have described the disturbances (spatial coherence degradation) of the atmospheric turbulence effects in coupling the laser beam with the SMF. The incorporation of adaptive optics to mitigate these effects is addressed. The coupling efficiency is improved using the Zernike model adaptive optics and the results are numerically evaluated. Various assumptions related to the atmospheric strength are made and the results are obtained for corrected polynomials in simulation [8]. Wei Liu et al. have presented the significance of beam pointing in FSOC in terms of BER, pointing error probability density function (PDF), and intensity displacement on a focal plane. The fast steering mirror (FSM) is used to correct the displacement error using the parallel controller developed in FPGA. The minimum BER of 10⁻⁹ is achieved. The experiment is conducted in an indoor laboratory setup consisting of a controlled (man-made) turbulence simulation box. The digital signal processor (DSP) is jointly used with FPGA to generate the beam steering control signal [9]. F. Gago et al. have explained the tip-tilt mirror control based on the FPGA technology for adaptive optics system and reported that the FPGA is the best viable platform for the control process when a huge amount of parallel processing is needed. The experiment is conducted with integer and floating point calculations. The results are presented and analyzed. ChipScope tools are used to avail the auxiliary modules in the FPGA. The entire control setup is assembled on the optical breadboard inside the laboratory and the experiment is conducted [12]. Digital architectures developed in the FPGA for optical wavefront correction are described by K. Kepa et al. The design of the low-cost adaptive optics control system architecture is explained and the results are presented and analyzed. Mostly, a lookup table (LUT)based design is followed, and experimentation is carried out with some test pattern in the laboratory environment [15].

Nestor O. Perez-Arancibia et al. have developed the indoor beam stabilization system with the observerbased feedback controller. The disturbance is generated by the FSM and optical shaker and corrected by another FSM using the extended Kalman filter. The experimental results are presented and briefed. Separate computers are deployed for generating the disturbance (PC2) and control signal (PC1) since these algorithms are implemented in the software environment. Further, all the opto-electronic devices are mounded on an optical breadboard and the entire experiment is conducted inside the laboratory [16]. Wen-Fang Xie et al. have proposed a neural network-based adaptive controller for piezoelectric actuators (PEA) with unknown hysteresis. A neural network-based dynamic pre-inversion compensator is designed to cancel out the effect of the hysteresis. The results obtained from the simulation study are described; however, the experimental verification is required [20]. The complicated non-linear dynamics of PEA including hysteresis, creep, drift, and time delay are treated as a black box system by S. Yu et al. A neural network is built to compensate these behaviors to improve the beam positioning/tracking stability and accuracy. Experimental verification/validation for any specific application with PEA is required [21]. A neural network-based low-speed damping controller is designed to remove the non-linear disturbance in an operating stepper motor by Quy Ngoc Le et al. The backpropagation learning algorithm is used and the neural controller is implemented in the FPGA. The experimental results are investigated [22]. M.R. Suite et al. have explained the way of installing the FSM and OPD to correct the focal spot position fluctuation and thus reduce the power loss. The experiment is carried out across the bay (20-mile round-trip) at the Chesapeake Bay Detachment (CBD) of the Naval Research Laboratory (NRL). The calibration results of the OPD is given and the experimental results with and without active correction are explained. The experiment is conducted with the unmodulated optical beam, and only the performance improvement of the beam stability on the detector plane was studied [25]. Thus, designing an intelligent controller to resolve the non-linear and hysteresis behavior of the optoelectronic devices and building a low-power and compact hardware controller to generate a beam steering control signal by processing the beam position information become significant. Further, incorporating the developed control system in real-world open atmospheric FSOC data link and evaluating its greatest contribution by measuring and analyzing the typical communication parameters are also essential.

3 FSOC experimental test-bed configuration and control strategy description

The FSOC experimental test-bed (transmitter and receiver) as shown in Figure 1 is developed for the data link range of 0.5 km at an altitude of 15.25 m with the necessary opto-electronic components. The schematic diagram of the experimental setup is shown in Figure 2 that consists of a modulatable Beta-Tx optical source, optical shaker, data and disturbance sequence generator circuit (in FPGA), digital to analog converter (D/A), and transmitting optics at the transmitter. The receiver consists of a telescope, FSM, variable beam splitter, OPD, analog to digital converter (A/D), and neural controller (in FPGA). All the opto-electronic devices are mounted on the vibration-damped optical breadboards [16,19]. A serial pseudorandom binary sequence (PRBS) generator circuit of 2¹⁰-1 is

developed in the FPGA, and its bit stream output is given to the optical modulator at the asynchronous transfer mode (ATM) rate of 155 Mbps. A widely used UNRZ-OOK-IM-DD scheme, with a UNRZ signal of 0 V (low) for logic '0' and 3.3 V (high) for logic '1', is used to directly modulate the optical signal [4,7,9,10,23]. The modulated light is made to fall on the optical shaker and gets reflected towards the transmitting optics. The transmitting optics increases the beam diameter from 3 mm (i/p beam) to 9 mm (o/p beam), and the expanded beam is transmitted to the receiver through the atmospheric turbulent optical channel. An arbitrary disturbance sequence (12-bit resolution) generator circuit is also developed in the FPGA at the transmitter, and its corresponding analog voltage is given to the optical shaker on which the Pure Reflection Mirror (PRM) is mounted and it acts as the secondary possible source of jitter. The OPD and PEAs are the key devices that facilitate fast and precise beam steering to mitigate the beam wandering in the FSOC system. According to the influence level of the local atmosphere on the propagating optical wave, steering process requirements (optical feedback sensor, steering device, type/number of actuator, steering resolution, steering mirror aperture, control voltage, etc.) are chosen. The device identification, steady-state performance, and calibration analysis can be seen in our previous publication [19].

The telescope captures all the optical power and reflects to fall on the FSM. The FSM consists of a three-terminal PEA-based moving platform on which the beam steering mirror is mounted. The incident laser beam of the FSM gets reflected to the variable beam splitter that splits the incident light into two beams: reflecting beam and propagating beam.

The reflected beam is made to fall on the optical detector (photodiode) used for communication purposes. The photodiode generates a voltage related by a linear function with a negative slope to the intensity of light [16]. The propagating beam (passing through the beam splitter) is made to fall on the OPD. The OPD is constructed with four separate identical silicon photodiodes



Figure 1 Laser Communication Laboratory (LCL) facility. Photograph of the FSOC receiver (left) and transmitter (right) laboratories developed at existing the Information Technology (IT) block and tower (constructed for FSOC research work), respectively.

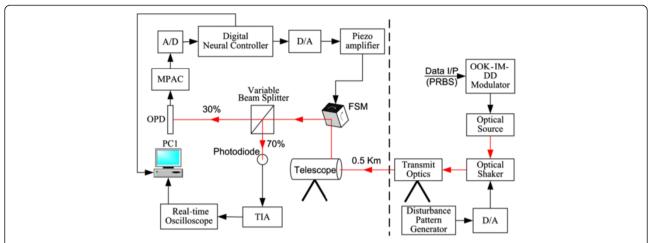


Figure 2 Schematic of the FSOC experimental test-bed for the 0.5-km data link. The receiver with the beam steering opto-electronic assembly (left) and the transmitter (right) are shown. The red arrow line indicates the optical path and the black arrow line the signal path.

denoted by A, B, C, and D and arranged in a quadrant geometry [19,25]. The output voltages of the OPD $(V_{\rm A}, V_{\rm B}, V_{\rm C},$ and $V_{\rm D})$ are given to the mono-pulse arithmetic circuit (MPAC). The MPAC is constructed using operational amplifiers for accomplishing the addition and subtraction of the signal as given in Equations 5 and 6. The beam spot (centroid) displacement errors $V_{\rm Ex}$ and $V_{\rm Ey}$ along the x and y channels (2D plane) of the OPD are measured as the relative output voltage changes by [19,25]

$$V_{Ex} = \{ (V_A + V_C) - (V_B + V_D) \};$$

$$V_{Ey} = \{ (V_A + V_B) - (V_C + V_D) \}$$
(5)

The reference signal $V_{\rm Ref}$ is measured by the algebraic sum of all the signals from the quadrants of the OPD [19,25] as in Equation 6.

$$V_{\text{Ref}} = (V_{\text{A}} + V_{\text{B}} + V_{\text{C}} + V_{\text{D}})$$
 (6)

The outputs of Equations 5 and 6 vary from -10 to +10 V and from 0 to +10 V, respectively. These signals are applied to the 12-bit parallel data-fetching A/D (AD1674 converter core) through an eight-channel analog multiplexer (ADG509A) circuit. The digitized outputs are given to the controllers via a very high density cable interconnect (VHDCI). The information about the beam position (displacement) on the OPD (i.e., beam wandering data) are the key inputs to beam wander mitigating control system and are acquired continuously from the intensity feedback signal as shown in Figure 2. The important statistical values related to the beam displacement on the OPD are estimated using the following equations.

Azimuth and elevation distance are measured in mm by

$$x_{\text{dist}} = -2(V_{\text{Ex}}/V_{\text{Ref}}) \; ; \; y_{\text{dist}} = +2(V_{\text{Ey}}/V_{\text{Ref}})$$
 (7)

Radial distance is measured in mm by

$$\gamma = \sqrt{\left(x_{\rm dist}\right)^2 + \left(y_{\rm dist}\right)^2} \tag{8}$$

The feasible ranges of error and control parameters are taken from the manufacturer limitations. The PEA exhibits inherent non-linearities such as creep and hysteresis [19-21,26]. The zero-friction piezo drives and flexure guidance allow sub-nanometer resolution and sub-microradian angular resolution. The hysteresis characteristics and step response of PEAs are generally nonlinear and usually unknown [20,26]. This non-linear behavior limits system performance via undesirable oscillations and instability. The non-linear hysteresis behavior of PEAs is tested, and the mere inspection gives that the steering goes to the saturation, inverse and dislocated effect, and non-linear and distinctly asymmetric response [19]. The complexity in control of beam steering arises due to their geometrical configuration, the physical phenomena present in the PEA operations, and other variables involved in its operation. The non-linear static input-output mapping of the system is not one-to-one [16]. Therefore, it is difficult to operate at an accurate trajectory using conventional controllers and a feed-forward neural network is put forward to resolve it [19-21]. Further, the conventional controllers could not be sufficient and the neural controller can be used for improving non-linear input-output mapping through which the beam wandering is mitigated and is the main contribution in this paper. The beam spot displacement error values are rescaled to lie within a range of -1 to +1. The rescaling (normalization) is accomplished by the linear interpolation formula given in Equation 9.

$$\sigma_{Ex} = \frac{(2048 - ((V_{Ex} + 10)/0.00489))}{(((V_{Ref} + 10)/0.00489) - 2048)}$$

$$\sigma_{Ey} = \frac{(((V_{Ey} + 10)/0.00489) - 2048)}{(((V_{Ref} + 10)/0.00489) - 2048)}$$
(9)

where σ_{Ex} and σ_{Ey} are the normalized error values of displacement error on the x and y positions, respectively. This normalization has the advantage of preserving exactly all relationships that do not introduce any bias. The error inputs and the corresponding control outputs are experimentally measured in the pilot survey using the developed experimental setup shown in Figure 2. Although there are many parameters that affect the beam steering process in beam stabilization, x and y displacement errors contribute the greatest effect on the success of its operation. Advantageously, these parameters can easily be measured during the closed-loop feedback control for beam steering operation with no additional cost and time [27]. These parameters are considered as the principal components in this work since they moreover directly affect beam stability and link quality. The neural controller output data (12-bit resolution) are converted to an analog signal using D/A and given to the FSM assembly through the piezo amplifier in a closed-loop feedback control. The beam position information, controller performance, demodulated data, and the quality metrics of data link are continuously monitored using the real-time oscilloscope and PC1.

4 Hardware architecture design and implementation of the neural controller

For on-chip training, the hardware platform suffers several disadvantages such as achieving high data precision, high hardware cost of calculations, development time, and flexibility of the platform as compared to the software [28-30]. At present, most of the neural controllers are simulated by software programs and implemented in a hardware platform due to the involvement of more computations and complicated arithmetic calculations in neuro-controller design. The FPGA or applicationspecific integrated circuit (ASIC) fabrication technology is more popularly being used due to the advantages of low power, compactness, huge amount of pipelined parallel data processing, and high speed computations [28,30]. Therefore, the neural controller weights and bias values are obtained from the MATLAB environment as a starting point for hardware implementation. The number of hidden layers and neurons is determined through a trial and error method in order to accommodate the converged error within the goal. The neural network training algorithm, behavior of learning function, and development of the neural controller can be seen in our previous publication [19]. The 2-12-9-2 (2 neurons in the input layer (IL), 12 neurons in first hidden layer (HL1), 9 neurons in second hidden layer (HL2), and 2 neurons in the output layer (OL)) is the structure of the developed neural controller as shown in Figure 3. The fundamental mathematical equations related to the feed-forward multilayer perceptron design with backpropagation learning algorithm can be found in section III of [22].

One of the trained patterns of the neuro-controller network structure is shown in Figure 3. A novel pipelined parallel architecture is developed in Xilinx FPGA and the neural controller is implemented. The ability of FPGA to perform massive parallel processing increases the obtainable control loop frequency, reduces the computational latency in the control system [15,22], makes the controller stand-alone, and operates at high speed [28]. The FPGA gives great flexibility in prototyping, designing, and developing complex hardware high gate density and many features necessary for neural controller implementation. The mixed design environment, very high speed integrated circuit hardware description language (VHDL) and Xilinx system generator, is used together since it simplifies the development of the neural controller and it is possible to model and simulate a digital system from a high level of abstraction module designs [31].

The global block diagram of intact digital architecture developed inside the FPGA is shown in Figure 4, and it consists of various main data processors and control engines. All the units/modules are developed to operate in parallel with the controlled data and command flow. The finite-state machine engine control information provides a command signal that coordinates and executes various operations in the data processor section in order to accomplish the desired data processing task. The digital circuits act as the controller that provides a time sequence of signals for initiating the operations in the data path and also determine the next state of the control sub-system.

A pipelined parallel architecture is built for accomplishing the necessary computations as per the neural controller algorithms. The pipeline level and the schedules of neural controller computation process flow are given in Figure 5, and the pipeline stages are marked by lowercase letters (a, b, c,..., g) in Figure 4. As can be seen in Figure 5, the operations are being performed at every moment. The feed-forward data flow is controlled by the pipeline stage control signal.

The developed novel architecture is divided into seven main blocks which are marked by uppercase letters (A, B, C,..., G) in Figure 4, namely A) clock manager unit, B) signal digitization and data processing unit, C) weight and bias memory management circuit, D) neuron unit, E) data routing and ring circuit, F) multiply-accumulator

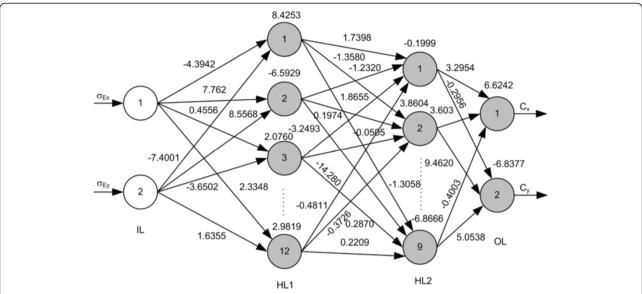


Figure 3 Trained pattern of the neural network. Typical backpropagation of the neural network pattern coded with weights and bias values for stand-alone linear time-invariant (LTI) controller.

unit, and G) serial communication manager, and are described in the following sub-sections:

4.1 Clock manager unit (A)

The on-board clock frequency 'm_clk' in the FPGA development board is 100 MHz. To achieve the required frequencies, the new clock signals have been synthesized by means of a digital clock manager (DCM) provided by

the FPGA. The block diagram of the clock manager module is shown in Figure 6a. The DCM output is given to the (i) internal shift controller, (ii) internal process controller, and (iii) enable signal generator. In these modules, starting from the DCM output, the required enable signals, shift control clocks, process control signals, command signals, data forward signals, and baud rate clock etc. have been generated at the specified

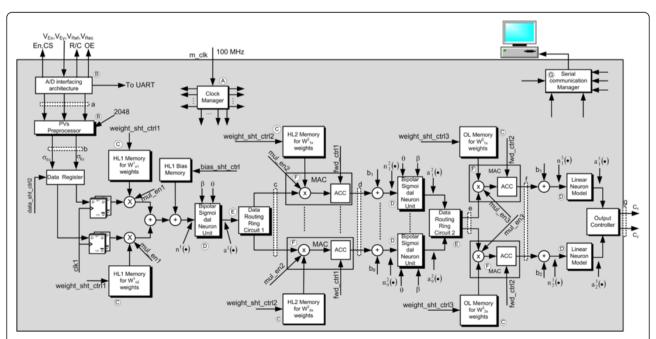


Figure 4 Global block diagram of clock manager, data acquisition, neural-controller and UART implementation in the FPGA device. A, B, C, D, E, F, and G are the main sub-circuits and a, b, c, d, e, f, and g are the pipeline stages.

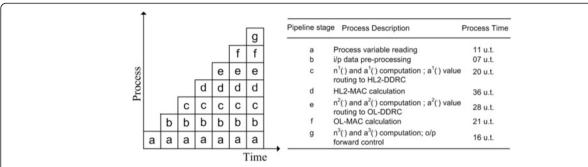


Figure 5 Example of pipelined process-timing diagram (brief) showing the computation process of neural controller with process description and time.

synchronized frequencies for globally controlled data flow and operations.

4.2 Signal digitization and data pre-processing unit (B)

This unit consists of two circuits, namely (i) A/D interfacing architecture and (ii) process variables (PVs) preprocessor. The A/D interfacing circuit is developed in the FPGA as shown in Figure 6b. The data required to enable (En) the analog multiplexer (MSB of MUX o/p) and Channel Select (CS) address (MSB-1: LSB of MUX o/p) are stored in the channel control register. The MUX routes the content of the channel control register in accordance with the present state of the 'ch_sel_ctrl' finite-state machine controller. The 12-bit output of A/D corresponding to the selected channel is forced to available at the input of the DMUX by asserting the Output

Enable (OE) control signal. The DMUX input is directed to the respective 12-bit wide register. The selective lines of the MUX and DMUX are synchronized for the proper operation with the finite-state machine. Once the content of all the registers are loaded, then the values are forwarded into the PVs pre-processor module. This action is accomplished by the command 'data_sht_ctrl1' from the finite-state machine. The PVs pre-processor performs the normalization operation as given in Equation 9, and the design flow graph is shown in Figure 6c. The radix-10 representation range of a 12-bit digitizer output is 0 through 4,095 with the center value of 2,048 for the 0-V input.

The $V_{\rm Ex}$ and $V_{\rm Ey}$ are compared with 2,048 (0 V) to identify the direction of the beam displacement, i.e., left or right on the x channel and above or below on the

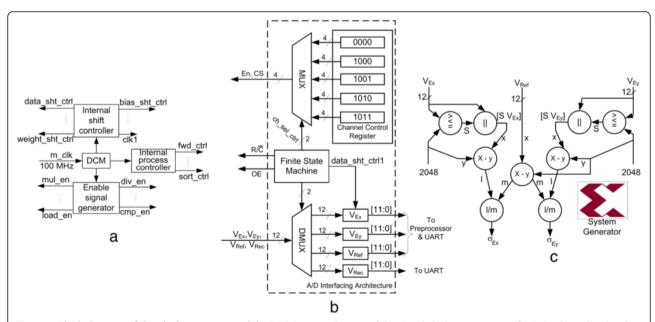


Figure 6 Block diagram of the clock manager module. (a) Schematic diagram of the digital clock manager unit. (b) Eight-channel and 12-bit parallel out bidirectional (-10 to +10 V) A/D interfacing and data acquisition circuit. (c) Hardware design flow graph of the data normalization algorithm in PVs pre-processor unit. Error signals $V_{\rm Ex}$ and $V_{\rm Ey}$ variations are normalized with respect to $V_{\rm Ref}$. An error signal of 0 V is equal to 800 H = (2,048)₁₀.

y channel, and the sign bit 's' is concatenated with the values of V_{Ex} and V_{Ey} with respect to the decision of the comparator. To measure the inner scale magnitude of the beam displacement on the OPD, 2,048 is subtracted from the values of V_{Ex} , V_{Ey} and V_{Ref} and then the results of V_{Ex} and V_{Ey} are divided by the result of V_{Ref} , so that the V_{Ex} and V_{Ey} are normalized with respect to the V_{Ref} . The normalized values of PVs σ_{Ex} and σ_{Ey} are loaded into the data register and forwarded to the D-FFs array through the data register. The content loading and forwarding to/from data register are performed by the control signal 'data_sht_ctrl2' as shown in Figure 4. The O(t + 1) = O(t) for the rising edge of the 'clk1' and this state is maintained till accomplishing inputs and synaptic weight multiplications followed by the addition of bias for the HL1 computations in a single-precision data format [32]. The next rising edge of the 'clk1' is applied to read and forward the subsequent inputs for HL1 computations.

4.3 Weight and bias memory management circuit (C)

The synaptic weights and bias values in the single-precision floating point format are stored in the RAM: W^1_{x1} , W^1_{x2} , and b^1_x for HL1; W^2_{1x} , W^2_{2x} , W^2_{3x} ,... W^2_{8x} , W^2_{9x} , and b^2_x for HL2; and W^3_{1x} , W^3_{2x} , and b^3_x for OL. The organization of weight and bias memory is shown in Figure 7, and the addresses are allocated based on the priority of data sequence forwarding for successive computations.

The RAM units are constructed as a circular data shift register, so that it forwards the chosen weight and bias values to the feed-back path as well as to the multiplier in the feed-forward path [30]. Three 12-element row vectors, nine 12-element row vectors with one 9-element column vector, and two 9-element row vectors with one 2-element column vector are the structure of the HL1, HL2, and OL memory, respectively. The input, synaptic weight, and bias value shifting are synchronized with the clock manager units that are controlled by the 'weight_sht_ctrl1' and 'bias_sht_ctrl1' signal for HL1, the 'weight_sht_ctrl2' and 'bias_sht_ctrl2' signal for HL2, and the 'weight_sht_ctrl3' and 'bias_sht_ctrl3' signal for OL. The weight and bias values are serially shifted to perform the input-weight multiplications, cumulative and bias addition operations to compute the net input of neuron ' $n^1(.)$ ' in HL1 and the weight are serially and bias are paralleley shifted to perform the multiply and accumulation and bias addition operations to compute the neuron net inputs ' n_1^2 (.) to n_2^2 (.)' and ' n_1^3 (.) and n_2^3 (.)' in HL2 and OL, respectively.

4.4 Neuron unit (D)

The neuron unit (activation function) is implemented to calculate the activation level of net input 'n' [28,33]. The

neurons in the HL1 and HL2 are bipolar sigmoidal activation functions and in the OL are bipolar linear activation functions. The bipolar sigmoidal activation function is normally modeled by the hyperbolic tangent function [28,30,33] which cannot be easily implemented in the FPGA since it consists of infinite exponential series [29]. The drawback of using an alternative method of lookup table for bipolar sigmoidal activation function implementation [30] is the need and utilization of a huge amount of hardware resources; therefore, it is implemented as a second-order non-linear function as in Equation 10 in FPGA, and various other methods of implementation of activation function can be found in literature [33].

$$a = f(n) = \begin{cases} 1 & \text{if } n \ge L \\ n(\beta - \theta n) & \text{if } 0 \le n < L \\ n(\beta + \theta n) & \text{if } -L \le n \le 0 \\ -1 & \text{if } n \le -L \end{cases}$$
(10)

where L and & – L are the upper and lower saturation limits, n is net input to the neuron, β is the slope of the model function, and θ is the gain of the model function. The digital architecture of neuron implementation using the Xilinx system generator (Xilinx block sets) is shown in Figure 8a. The net input 'n' is multiplied by the gain (θ) , and the multiplier output is forwarded to another two processes that adds and subtracts to/from the slope (β) . The results are given to the multiplexer which forward one of two inputs with respect to the selection input $(S_1: 0 = \text{first input}, 1 = \text{second input})$. The output of the first multiplexer is multiplied by the net input 'n' and goes to the second multiplexer which forwards one of three inputs depending upon the selection input $(S_2: 0 = \text{first input}, 1 = \text{second input}, 2 = \text{third input})$. The simulation results of real and second-order non-linear bipolar activation functions for the input range of (-255, 255) are shown in Figure 8b, and the important observations are (i) the response of the second-order non-linear model precisely fits with the real model; (ii) the input range, slope, gain, and upper- and lower-limit parameters can be varied based on the application; and (iii) the possibility of Xilinx block set-based effective hardware implementation. Only one neuron is implemented instead of 12 neurons in the HL1, and full activation-level computations are accomplished by the cyclic shifts of inputs, weight, and bias $(W_{x1}^1, W_{x2}^1, \text{ and } b_x^1)$ and the input and output of the neuron are denoted by ' $n^1(.)$ ' and ' $a^1(.)$ ', respectively. In the HL2, 9 neurons are implemented and the input and output are denoted by $n_1^2(.), n_2^2(.), ..., n_9^2(.)$ and $a_1^2(.), a_2^2(.), ...$ a_9^2 (.), respectively. The OL consists of 2 neurons and the input and output are denoted by $n_1^3(.)$ and $n_2^3(.)$ and $a_1^3(.)$ and $a_2^3(.)$, respectively.

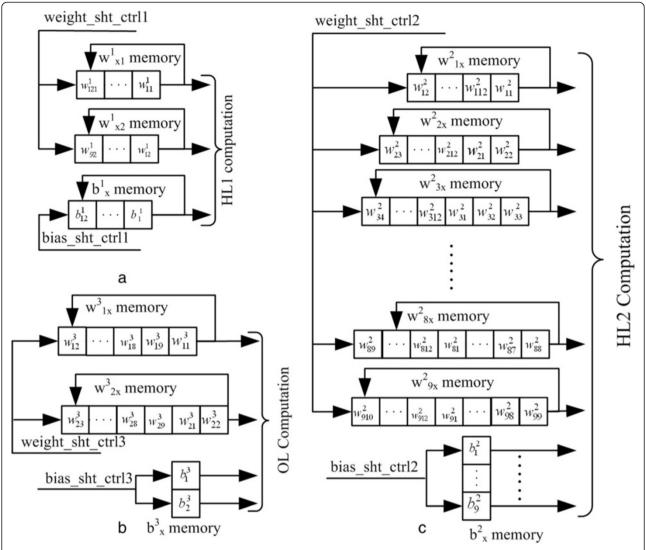


Figure 7 Organization of weight and bias memory. Synaptic weight and bias value memory organization in single-precision (32-bit) floating point data format in RAM for (a) the first hidden layer (HL1), (b) the output layer (OL), and (c) the second hidden layer (HL2).

4.5 Data routing ring circuit (E)

Two data routing ring circuits (DRRCs) are designed and used in such a way as to utilize the minimum amount of hardware resources to feed the data to the multiply-accumulation unit as a serial-in serial-out circular shift register (SISOCSR) for the HL2 and OL configuration as shown in Figure 9a,b. The DRRC units are developed based on the methodology of neuron configuration, i.e., one neuron or multiple neurons. Since one neuron is implemented in HL1, a 1×12 demultiplexer is used in the first DRRC to sort the input value into the corresponding second input of a 2×1 multiplexer, i.e., $a^1(.)$ is demultiplexed to $a^1_1(.)$, $a^1_2(.)$, $a^1_3(.)$,... $a^1_{12}(.)$ as shown in Figure 9a, and this sorting is accomplished by the command selection line 'sort_ctrl' signal. Initially, the selection line of a 1×2 multiplexer 'load_en1' is set

to '1'. Therefore, the sorted data are available at the input of the SISOCSR; otherwise, the 1×2 multiplexer output depends on the first input, i.e., the output of the previous register.

As soon as one set of sorting is over, the register clock 'rot_ctrl1' is applied and then the register outputs are available at the first input of 1×2 multiplexers. At this time, the 'load_en1' is set to '0', so that one circular shift is accomplished as $a_{12}^1(.)$, $a_1^1(.)$, $a_2^1(.)$, $a_3^1(.)$, $a_4^1(.)$, $a_5^1(.)$, $a_6^1(.)$, $a_9^1(.)$, $a_{10}^1(.)$, and $a_{11}^1(.)$. These cyclic rotations are continued for 12 subsequent clock inputs and then repeated with a new set of input data. The first nine register outputs are given in parallel to the HL2 multiply-accumulation computations. The outputs of the HL2 neurons $a_1^2(.)$, $a_2^2(.)$, $a_3^2(.)$, $a_4^2(.)$,... $a_9^2(.)$ are directly given to the second input of the 1×2 multiplexer of OL

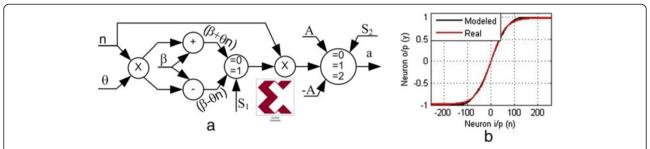


Figure 8 Digital architecture of neuron implementation using the Xilinx system generator. (a) Hardware design flow graph of the hyperbolic tangent sigmoidal (bipolar) activation function model as the second-order non-linear function and (b) plot of real and modeled neuron behaviors with $\sigma = 0.032$, $\theta = 1$, $\beta = 255$, $n \in \{-255, 255\}$, and $L = \pm \beta/2$.

DRRC as shown in Figure 9b. The 'load_en2' is set to '1'; therefore, the inputs are available at the input of the registers. The register inputs are shifted to the next stage when the clock 'rot_ctrl2' is applied and the status becomes $a_9^2(.)$, $a_1^2(.)$, $a_2^2(.)$, $a_3^2(.)$,... $a_8^2(.)$, and at this time, the 'load_en2' is set to '0'. These cyclic rotations are continued for 9 subsequent clock inputs and then repeated

with a new set of input data. The first two register outputs are given in parallel to the OL multiply-accumulation computations.

4.6 Multiply-accumulator unit (F)

The two main factors considered during the hardware implementation of Multiply-ACcumulator (MAC) units

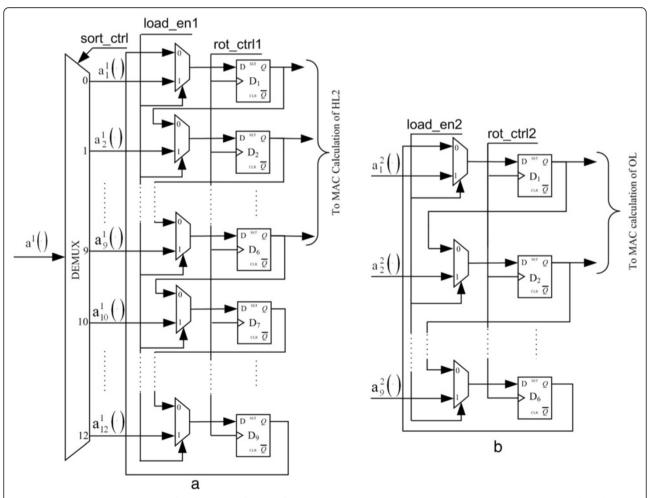


Figure 9 Data routing ring circuits for the HL2 and OL configuration. Neuron output data routing ring circuits and serial-in and serial-out circular shift register array to accomplish the multiply-accumulation computation for (a) the second hidden layer (HL2) and (b) the output layer (OL).

are (i) need of reasonable precision and (ii) cost of more logic area associated with precision [30]. The singleprecision (32-bit) floating point arithmetic standard is used for accomplishing the input and synaptic weight multiplications with bias additions and all the arithmetic operations [32]. The two modules of the MAC unit architecture are (i) multiplication and (ii) result accumulation. The design flow graph of the MAC circuit is shown in Figure 10. The nine MAC units for HL2 and the two MAC units for OL are developed for neuron inputs $n_1^2(.)$ through $n_2^2(.)$ and $n_1^3(.)$ and $n_2^3(.)$ computations. The first MAC unit section multiplies the outputs of the first DRRC with the corresponding weights and is accumulated. The weight values and DRRC output shifting are controlled and synchronized by the internal shift controller unit. The command 'mul_en' signal ensures the availability of DRRC outputs and respective weight data and triggers the multiplication process. In accumulation, the multiplier output 'au' is added with the previously accumulated value 'ad' and the result 'sum' is stored in a register for future accumulation. Once one MAC operation for one complete set of inputs is accomplished, the final result is forwarded to the bias addition in parallel for the rising edge of command 'fwd-ctrl' signal so that the final output, i.e., the inputs to the HL2 neurons $n_1^1(.)$ through $n_2^1(.)$ are ready. Similarly, the second MAC unit section multiplies the outputs of the second DRRC with the corresponding weights, accumulates, and finally forwards to the bias addition in parallel, so that the OL neural inputs $n_1^3(.)$ and n_2^3 (.) are ready. The OL neuron outputs are given to the D/A circuit.

4.7 Serial communication manager (G)

The Universal Asynchronous Receiver Transmitter (UART) RS232 standard communication protocol is implemented as a separate digital architecture in the FPGA as shown in Figure 11a. The output of the MUX1 is forwarded to the parallel-in serial-out shift register (PISOSR) and sends 1 bit at a time to the MUX2 for the rising edge of the 'clk_sig' signal. The output of the mux2 'txd' is 'sdata(0)', i.e., LSB of PISOSR, when the selection line 'mux_sig' is set to '0'; otherwise, the stop bit '1'. The baud rate counter

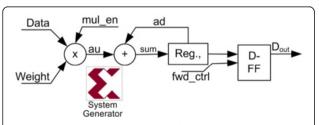


Figure 10 Multiply-accumulation architecture implementation design flow graph.

generates the bit transmission clock, i.e., baud rate clock 'clk_sig' at the rate of 9,600 from the master clock 'm_clk' signal.

The transmission of the measurement (M/m) data bit at the PISOSR and the stop bit are controlled by the bit shift controller in accordance with the 'clk sig'. Further, the bit shift controller conveys the status of the frame transmission to the byte shift controller using 'cnt2' that switches the selection line of MUX1 'cnt3' to choose the next channel (frame). Once all the frames of M/m data corresponding to one sampling cycle are transferred, then the byte shift controller enables the data buffer to read the new set of M/m data by the command 'data rd' and continues. In order to avoid the occurrence of communication conflict among the frames, two header (H1 and H2) frames are transferred followed by the M/m data frames and one footer (F1) frame for the appropriate coordination among the data, so that a total of 11 frames need to be transferred for every data acquisition cycle as shown in Figure 11b. A computer (PC1) is used to log all the M/m data to perform the on/off line computations related to the experimental data analysis.

5 Experimental results and data analysis

The developed neural controller is installed at the FSOC receiver experimental setup as an observer-based control for beam stabilization. The beam wandering mitigation experiment using the developed neural controller is conducted in different local weather conditions (monsoon, rainy, winter, pre-summer, and summer) in a period of 1 year. A highly accurate weather station is built [6] and used to continuously measure the local weather changes in diurnal periods. The measurements corresponding to the weather changes are stored in the data-logging computer. The results presented below are corresponding to the winter session (15 December 2013 - Sunday). In this season, the weather parameter variations from 1.5 to 5.1 ms⁻¹ with the standard deviation (Std) of 0.97 ms⁻¹ for wind speed (Ws), 23°C to 31°C with the Std of 2.65°C for temperature (T), 52% to 94% with the Std of 13% for relative humidity (RH), and 1 to 4 km with the Std of 0.87 km for visibility (V) are observed. The Std of T and RH are high while those of Ws and V are low. The different conditions of the atmosphere observed on 15 December 2013 (Sunday) are hazy, with scattered clouds, misty, foggy, and partially cloudy. The disturbances are introduced in the beam propagation angle for the frequency range of 0 to 2 kHz at the transmitter in addition to the turbulent channel effects to validate the maximum capability of the developed closed-loop neural-control system. The performances of the developed neural controller are intensively investigated in a closed-loop control configuration. Some of the important data experimentally acquired in real time are presented, and from them, the potential

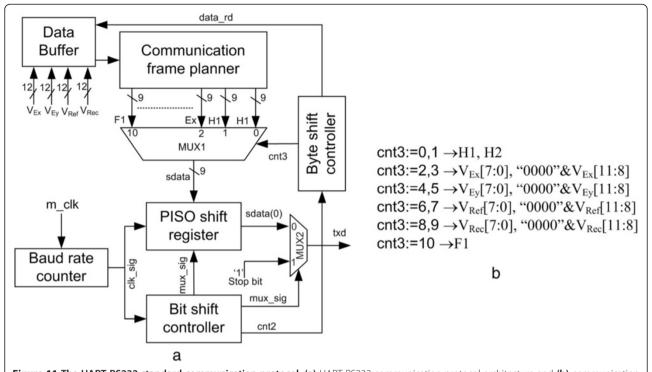


Figure 11 The UART RS232 standard communication protocol. (a) UART RS232 communication protocol architecture and **(b)** communication frame format.

and feasibility of the proposed neural controller are discussed. The outstanding performance of the neural controller in mitigating the beam wandering and reducing the received optical signal fluctuation is analyzed. The significance of the proposed controlling scheme in improving the reliability of the FSOC data link is evaluated, and the results are presented in this section.

5.1 Performance study of closed-loop experiment with intensity feedback control

The maximum performance of the controller could not be arrived at in an open-loop control configuration since it depends on the following: (i) accuracy of the estimation of the position errors using the OPD, (ii) long-term behavior of opto-electronic components, (iii) greater number of PEA motion cycles, (iv) surpassed magnitude and phase response (sensitivity) of the FSM, (v) achievable neural controller performance in the LTI control scheme, (vi) sensor noise, and (vii) initial LoS alignment. Therefore, the intensity feedback (as observer)-based closed-loop control configuration becomes significant. In the identified system considered in this work, the optimum values are $Cx^* = 0.2157 \text{ V}$ and $Cy^* = -0.1634 \text{ V}$ and these two values are very important in all the experiments. As a direct consequence of the beam wandering mitigation (disturbance rejection) in each channel, the ensemble average value of the position errors are significantly closer to (0,0)mm. The test experiments to analyze the improvements due to the neural controller in the closed-loop control configuration to the disturbances are conducted, and samples of the results are shown in Figure 12. It can be seen that the greater performance improvements are attained once the neural controller is turned on.

The obtained min-max values of beam centroid wandering in the no-control condition are -1.73 to +1.71 mm, whereas in the control condition, the values were -0.13 to +0.16 mm for both channels. The statistical results show that the neural controller in a closed loop generates the accurate control signal as required to mitigate the beam wandering.

The power spectral density (PSD) is computed for the time series data to analyze the disturbance rejection as the function of frequency and shown in Figure 13. The disturbance to the x channel has a spectrum-wide low-frequency content in the range 0 through 2 kHz with two narrow bands approximately at 0.48 and 1.12 kHz. The correction input to the FSM has a frequency of 2 kHz. The PSD results show that the proposed control scheme is capable of rejecting disturbances in the range 0 through 2 kHz. The PSD greatly demonstrates that the disturbance band is attenuated in the x channel by a maximum of 45 dB as in Figure 13. The PSD of the spot motion indicates that most of the frequency content fall in the range of 0.45 to 0.85 kHz. A similar behavior is reported for the y channel. In the y channel, the disturbance

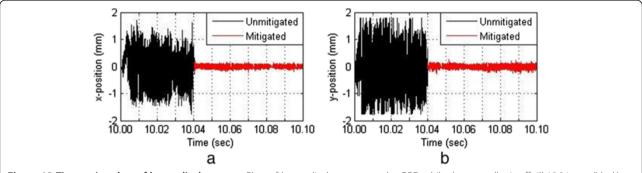


Figure 12 Time series plots of beam displacement. Plots of beam displacement on the OPD while the controller is off till 10.04 a.m. (black) and on from 10.04 a.m. onwards (red) for **(a)** *x* and **(b)** *y* channels.

band is attenuated by a maximum of 55 dB approximately. The disturbance given to both channels has a spectrum composed of narrow band disturbances. Almost the same observations are commanded for a longer period in different weather conditions; the disturbance at the frequency range 0 through 2 kHz had been effectively rejected. Further, the results show that the neural controller is capable of significantly attenuating the disturbance affecting both channels. In this case, what is interesting to notice is that the overlapping frequency bands are noticeably attenuated, however, not as much as in the cases in which the frequency bands do not overlap due to cross interference between both channels as commented in literature [16,21].

5.2 Analysis of beam spot auto-alignment and reduction of wandering

Optical beam angular deflections along the propagation path wander the beam randomly out off the LoS between the optical source and detector. The instantaneous center of the beam, i.e., the point of maximum intensity, is randomly moving on the detector plane. The performance improvement in beam stabilization through the beam steering control system is tested in controller tuned on and tuned off conditions. The beam centroid

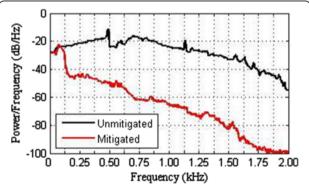


Figure 13 Comparison of PSD of time series position data acquired with no control and control for the *x* channel.

coordination on the 2D plane of the OPD is estimated using Equation 7, and a portion of data is shown in Figure 14a: with beam steering off (blue), beam steering on (red), and optimal value (black). The following are the interesting observations from Figure 14a in no control: (i) beam centroid wanders in almost all the areas of the OPD plane, (ii) centroid movements are highly random, (iii) sometimes the centroid goes out off the communication detector plane, i.e., the communication is disconnected, and (iv) the centroid shows a wide range of power fluctuations at the communication detector.

In the control are the following: (i) centroid movements are controlled and always around the optimal point, (ii) a very narrow range of power fluctuation is seen, and (iii) the maximum intensity of the beam (Gaussian beam) is concentrated at the center of the communication detector. The radial distance of the beam centroid on the OPD is calculated with respect to (0,0)mm using Equation 8, and the corresponding histogram plot is shown in Figure 14b: in no control (blue), in control (red), and optimal value (black) which evidences that the beam steering control system mitigates the beam wandering and stabilizes the beam almost at the center of the communication detector. The received signal magnitude is significantly improved and close to the optimal magnitudes in the presence of beam steering control, increases the reliability of the FSOC link, and maintains the stable SNR to decrease the BER. The average received signal magnitude is 0.0172 V for the 0-V (logic '0') input due to sensors and circuit noise. The radial displacement distance is divided into six regions and denoted by the linguistic terms VS (0 to 0.5 mm), S (0.5 to 1 mm), M (1 to 1.5 mm), H (1.5 to 2 mm), VH (2 to 2.5 mm), and VVH (2.53 mm) where VS is very small, S is small, M is medium, H is high, VH is very high, and VVH is very very high.

5.3 Behavioral study of scintillation and communication signal quality metrics

The (0,0)V outputs from the OPD means that the beam centroid is positioned on the center of the photodiode

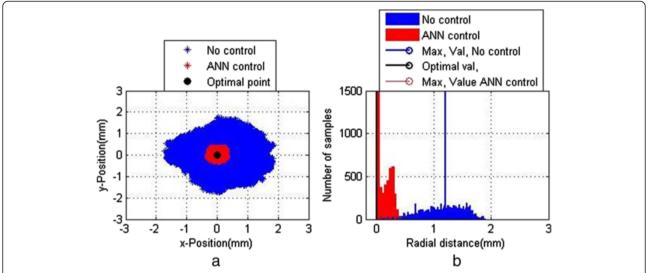


Figure 14 Laser beam spot centroid motion with and without beam steering control. (a) Beam wandering on a 2D-4Q plane with horizontal and vertical scales of real space. (b) Histogram of the beam centroid radial distance.

(communication detector) and its output is exactly minimum possible value, i.e., should coincide with the lower bound of the photodiode output $V_{\rm Rec}^*$ =0.3162 V. In the absence of sensor and circuit noise, the photodiode output difference at a given time $(V_{Rec}(t) \sim V_{Rec}^*)$ measured in volt is directly related to the atmospheric turbulence effects: scintillation and bam wandering. This beam wandering effect is mitigated using the developed beam steering system, so that the beam stability (maximum intensity) at a particular point on the photodiode is significantly improved. The power fluctuations of the received signal due to beam wandering are evaluated with and without the beam steering control system. The ensemble average of the optical power is used to estimate the ESI: power fluctuation due to beam centroid wandering, using Equation 1. The results corresponding to the 2,000 ensemble averages computed for control off and on conditions are shown in Figure 15a,b, respectively. ESI ≤1 is corresponding to the VS and S and ESI >1 is corresponding to the M through VVH regions. For lower values of ESI, the PDF distribution is nearly Gaussian centered about $I_0/\langle I \rangle$ value of 1. As ESI increases, the PDF is more skewed with a long tail towards the infinity and reduces peak intensity as a result of signal fading [1,4,10].

It is clearly reported from Figure 15 that the ESI fluctuates within broader variations (in the outer scale) from 0.014 to 1.86, i.e., 0.73% to 97.65% are seen when the steering is turned off. The variations in the inner scale with the min-max values of 0 and 0.15, i.e., 0% to 7.87%, are absorbed when the beam steering is turned on. These results exhibit the efficiency of the neural controller in steering the beam as required. Therefore, the neural controller in a closed loop improved the reliability of the FSOC data link. The ESI fluctuation, even with the beam steering turned on condition, reaches the maximum value of 0.15. This is due to a purely optical power fluctuation in the transmission path due to scintillation of the refractive index of the channel (Mie/Rayleigh scattering, absorption and particle interactions with the optical beam, etc.)

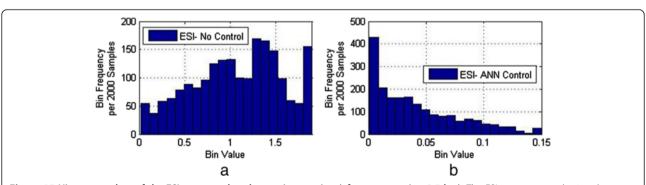


Figure 15 Histogram plots of the ESI computed at the receiver station (after propagating 0.5 km). The ESI was computed using the ensemble average of irradiance of the optical signal with the beam steering turned off (a) and on (b).

which could not be controlled by the steering system, but data coding and/or suitable modulation techniques developed for modern digital communication system can be used to solve it significantly [2,4,10,13,14,23,24]. However, this is the matter of separate research and out of the scope of this paper. As a direct consequence of the disturbance rejection in each channel, the average value of the photodiode output is significantly closer to the optimal value V_{Rec}^* , despite the fact that $\{\sigma_{\text{Ex}}(t), \sigma_{\text{Ey}}(t) \text{ and } Cx(t), Cy(t)\}$, $\forall t$.

The beam is modulated by the PRBS data stream at the ATM rate of 155 Mbps. The quality of the data transmission in the FSOC link is measured in a daylong operation to study the stability and reliability of the communication system. The communication metrics such as signal power, Q-factor, SNR, and BER values are continuously measured. All the measured values are stored in the data-logging computer. The Q-factor is measured as given in Equation 3 for different positions (S through VVH) of the beam centroid on the OPD; the corresponding theoretical BER is estimated using Equation 4 and shown in Figure 16. The Q-factor value linearly decreases and the BER increases with increasing the centroid radial displacement distance of the received beam. These results exhibit the importance of the beam stabilization in the FSOC system and lead that the received beam must be stabilized regardless of its AoA. The beam steering control system turned on and turned off conditions are alternatively done in the 1-min time interval, and the dependence of the BER with the O-factor is evaluated and the results are shown in Figure 17. The measured BER keeps close agreement with the theoretical BER. Note that the BER in Figure 17 is truncated to 6.46×10^{-9} . The variation range of BER in no control is from $9.324 \times$ 10^{-1} to 1.015×10^{-8} and in control is from 6.4516×10^{-9} to 1×10^{-8} which is less than 10^{-6} . Once the control is on, the received beam is stabilized so that the value of the Q-factor is improved and hence the BER comes down to

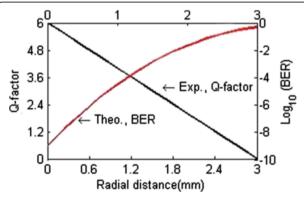


Figure 16 Experimental Q-factor and theoretical BER estimation against the beam centroid displacement on the OPD.

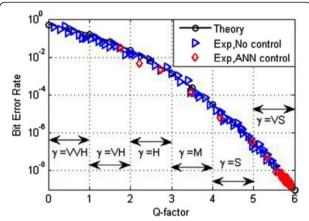


Figure 17 BER as a function of Q-factor. Theoretical (black) and measured BER with the beam steering feedback turned off (blue) and on (red) alternatively for every 60-s time interval.

below 10⁻⁸; otherwise, it falls in the upper regime. Furthermore, the BER reaches greater than 10⁻⁶ even with beam steering control in the beginning of measurement due to the pilot sequence synchronization scanning time, bit slip, and false detection in the real-time oscilloscope. As can be seen from Figure 17, a huge improvement compared to the no control experiments is demonstrated, the beam stability is improved, the outage probability is decreased, and the better BER is achieved without any forward error control (FEC) techniques.

The radial displacement distance values measured on 15 December 2013 for the diurnal period are subjected to generate the histogram plot to identify the most occurring sample values and their corresponding linguistic terms (S through VVH).

The most occurring sample values, linguistic terms, and minimum and maximum values of average BER are given in Table 1. The daylong measurements clearly demonstrate that the received beam centroid is retained within the VS region when the controller is turned on and the BER varies between 6.45×10^{-9} and 1.04×10^{-8} . The beam centroid wanders almost in all the regions when the controller is turned off, and the BER varies from 7.13×10^{-7} to 1.34×10^{-1} . Almost the same results

Table 1 Statistics of beam wandering and BER

High frequency sample (mm)	Radial distance linguistic	Average BER	
		Min	Max
0.143	VS	6.45×10^{-9}	1.04×10^{-8}
0.614	S	7.13×10^{-7}	7.81×10^{-5}
1.235	М	8.51×10^{-5}	5.31×10^{-3}
1.846	Н	5.83×10^{-3}	1.41×10^{-2}
2.314	VH	2.45×10^{-2}	6.25×10^{-1}
2.828	WH	6.79×10^{-2}	1.34×10^{-1}

have been reported in different weather conditions. Greater improvements in beam stabilization (coupling the power in the bucket to the communication detector) are achieved by the incorporation of the neural controller.

6 Conclusions

The significances of the received beam ATP system are reviewed. The most relevant literature survey results are briefed. The establishment of the 155-Mbps terrestrial FSOC data link for the range of 0.5 km at an altitude of 15.25 m with the necessary opto-electronic equipments is explained. The beam centroid displacement information is continuously obtained using the OPD and MPAC. The displacement and radial distance are estimated using the outputs of the MPAC. The optimal weights and bias (goal $\leq 10^{-6}$) values of the designed neural controller structure of the 2-12-9-2 multilayer perceptron model are found in the MATLAB environment. The pilot survey experimental data are used to train and test the neural controller's control signal prediction accuracy. A new design approach for the implementation of the neural controller in the FPGA is discussed. The architecture for implementing the UART RS232 standard communication protocol is developed as a separate digital architecture and used to transfer (store) the measurement/computational data to the computer (PC1) and to subsequently carry out on/off line data analysis.

The entire regions of the OPD are equally divided into six sub-regions, and the corresponding Q-factor and average BER values are measured and discussed. The FSOC performance improvements due to the beam wandering mitigation system are evaluated in controller turned off and on conditions. The values of the ESI are estimated and brought down to the controlled range of 0 to 0.15. The beam wandering range of -0.13 to +0.16 mm, maximum of 55 dB disturbance band attenuation with a frequency range of 0 Hz through 2 kHz, O-factor of 6, and BER of 6.45×10^{-9} are achieved due to the incorporation of the developed neural controller in different real-world environmental conditions. The results presented in this paper are intended for setting up the FSOC transceiver. So, it is suggested that the use of the neural controller for fine steering applications is best instead of complex/complicated computational algorithms found in literature. This control scheme can also be used in various applications like beam stabilization, steering, focusing, beam spotting, beam coupling and real-time control system, etc. A new version of the neural controller for deformable mirror control is also being implemented in FPGA and will be finished in the near future.

Competing interests

The authors declare that they have no competing interests.

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