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Channelized active noise elimination (CANE) for suppressing quantization noise in bitstream modulated transmitter (BMT)

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Abstract

Bitstream modulated transmitters may offer improved power efficiency and linearity simultaneously in RF power amplifiers. Several modulation techniques including envelop delta-sigma modulation and envelope pulse width modulation have been applied. The out-of-band quantization noise associated with these modulations may be rejected by a high-quality factor output filter, yet the in-band quantization noise needs to be further suppressed to meet the requirement of the emission mask. The proposed channelized active noise elimination technique can offer additional quantization noise suppression through software control without involving a passive filter. The essential concept is based on combining the outputs of multiple channels of Pas that have digitally controlled delays to form a FIR filter in analogue domain. A two-channel and a four-channel GaN power amplifiers are built to demonstrate this noise suppression concept and power combiners based on T-junction with quarter wavelength transmission line are proposed to retain the high power efficiency of the transmitters.

Keywords: Delta-sigma modulation, Pulsed load modulation, Pulse width modulation, Active noise filtering, Switching mode power amplifiers, GaN power amplifiers

1 Introduction

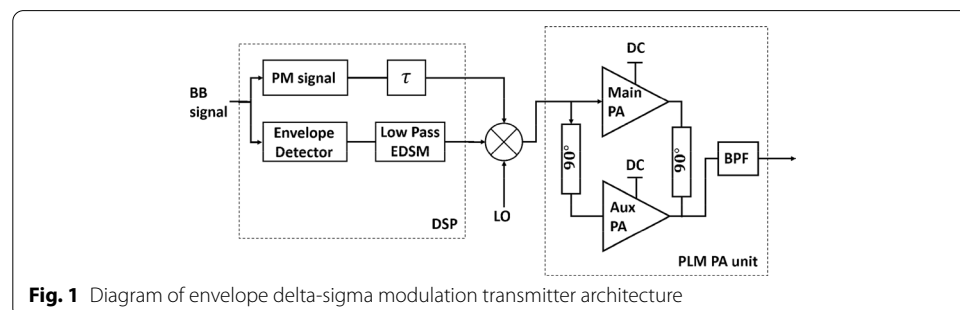
NEXT GENERATION wireless communication aims at achieving high speed data transmission with advanced signal modulation techniques such as QAM or OFDM for their high spectral efficiency. However, the increased peak-to-average power ratio (PAPR) of such modulations often requires the power transistors to operate at a significant back-off from its maximum output which compromises the overall power efficiency. Solutions to this problem include Doherty power amplifiers or envelop tracking (ET) techniques that can recover the power efficiency through either load modulations or supply modulations, while digital pre-distortion (DPD) is often leveraged to compensate for the nonlinearity. Bitstream modulated transmitters (BMT) have been proposed [1–11] as alternative approaches to yield high power efficiency in back-off cases while retaining the linearity of the transmitter without needing DPD. The essential idea of BMT involves the following three steps. The first step is to re-modulate the original RF signal and

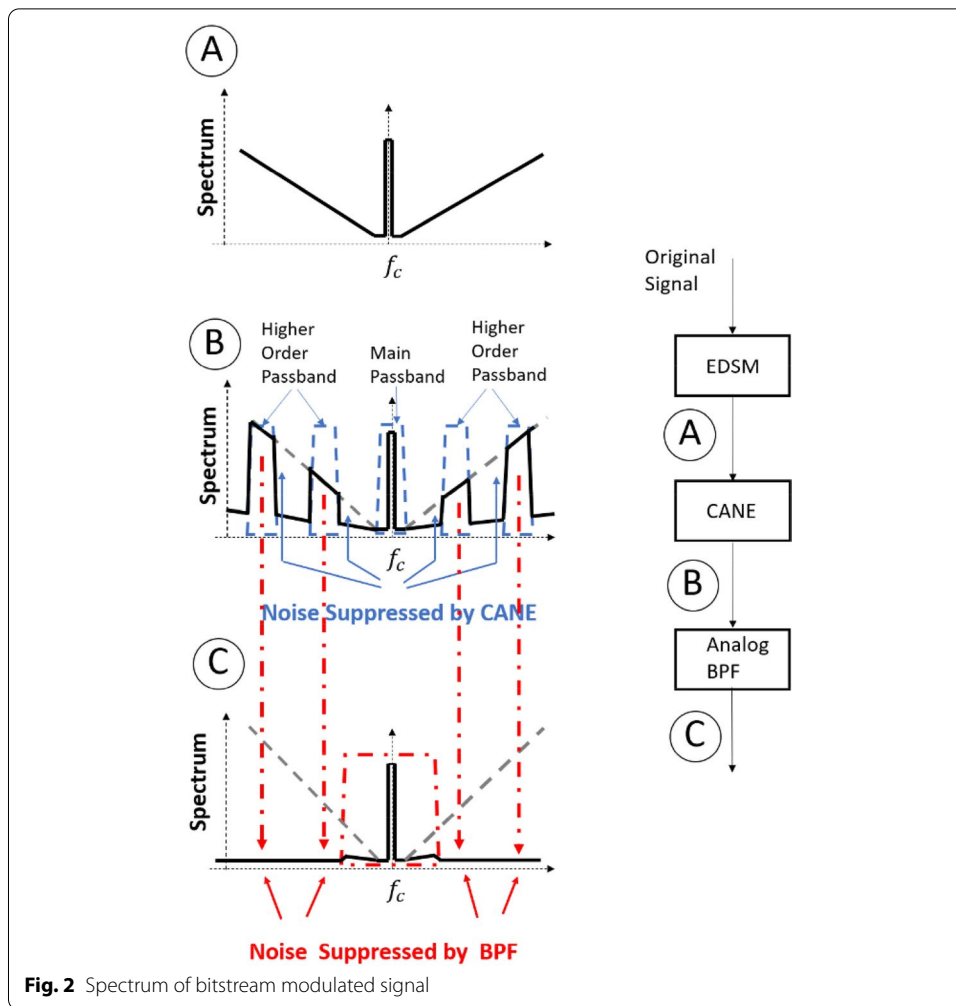
convert its non-constant analogue envelope to an envelope of bitstreams or pulses. Such modulations include pulse width modulation (PWM) [2] and envelope delta-sigma modulation (EDSM) [3–7]. The modulated signals are with discrete levels of magnitude, thus well suited for high efficiency amplification with switched-mode power amplifiers. The last step is to recover the original signal with analogue envelope through filtering out the quantization noise of the bitstream modulation.

BMT must work with either load modulation or supply modulation to gain the simultaneous benefit in both efficiency and linearity. For example, a pulsed load modulation (PLM) transmitter with EDSM was proposed in [7, 10, 11] as illustrated in Fig. 1. By pairing dynamically switching transistors with a high-Q output bandpass filter, a load modulation is formed so that the power of quantization noise is reflected to the supply and suppressed from the output. Comparing to the conventional Doherty amplifiers, the PLM PA offers a flat, optimal efficiency curve for up to 6 dB output power back-off. Multi-bit delta-sigma modulation techniques have also been employed by [9–11] to further improve the adjacent channel power leak ratio (ACLR) of such transmitters.

The suppression of quantization noise in BMT is a critical issue and it has been often accomplished with two complementary approaches. The first approach is through the noise shaping function of delta-sigma modulation which pushes the quantization noise away from the frequencies adjacent to the signal channel to the far-out frequencies. The second approach is to place a RF bandpass filter at the output of power amplifier (PA) to remove the far-out quantization noise outside its pass band. These two approaches, however, often cannot achieve a sufficient suppression to the quantization noise inside the filter passband but not immediately close to the signal channel, as shown in Fig. 2. Intuitively, one can either use filter with narrower bandwidth, or a higher-order multi-stage delta-sigma modulator with higher oversampling ratio. The former requires a filter with high-quality factor, which is difficult to implement in RF frequency. The latter may lead to an impractical complexity of the bitstream modulator.

An alternative approach called channelized active noise elimination (CANE) is proposed [12–14] to improve the noise suppression. CANE is an active noise filtering method through combining multiple channels of amplified signals with different time delays. Similar techniques have been discussed [15–19] by implementing a FIR filter in an analogue fashion with either digital or analogue delay lines directly inserted into the RF paths. As the time delay of each RF channel is translated into a periodically varying phase difference in term of frequency, combining the outputs of multiple channels forms periodically distributed pass bands and stop bands. By choosing appropriate delay





lengths, a higher-order pass band can be formed at the intended RF band. In these techniques, the delay lengths and combining coefficients determine both the bandwidth and the center frequency of the bandpass filter. Therefore, the selections of the bandwidth and the center frequency of the filter cannot be made independently. Also, the center frequency of the passband as a higher-order band is sensitive to the delay variation.

The novel contribution of this work is to implement CANE techniques directly in baseband through FPGA. Essentially, the low pass FIR filter is created in baseband and up-converted to RF to form a RF bandpass filter. This involves delaying the multiple channels of baseband signals with FPGA and up-converting them to RF with mixers before they are amplified and combined. Comparing to the analogue approaches [15–19], the digitally implemented CANE decouples the center frequency of the passband from the length of the delay line and is thus more robust to delay variation. Moreover, the delay of the multiple signal channels can be digitally generated at baseband without needing physical RF delay lines, which offers a true software-defined RF filtering solution to BMT quantization noise.

This paper is organized as the follows. Section 2 discusses the principle of CANE technique in detail, including the system concepts and the design of power combining

network that retains the power efficiency. Section 3 presents the implementation of a two-channel and a four-channel S-band PLM transmitters with GaN amplifiers and a FPGA-based digital controller for CANE. Section IV shows the measured results and discussions for future improvements.

2 Methods

2.1 Principle of Active filtering

The block diagram of a BMT with CANE is shown in Fig. 3. The original complex baseband signal is modulated by an EDSM modulator to a bitstream envelope fashion, and then, both the I and Q paths are split into multiple channels with different delays. These delayed signals are then up-converted with the identical local oscillator (LO), amplified and combined.

Let the normalized equivalent baseband filter impulse response be denoted by $h_B(t)$ and the corresponding filter transfer function by $H_B(f)$. To simplify the analysis, the combining coefficients C_k are assumed to be positive real numbers. Based on the block diagram in Fig. 3, $h_B(t)$ and $H_{RF}(f)$ are given by

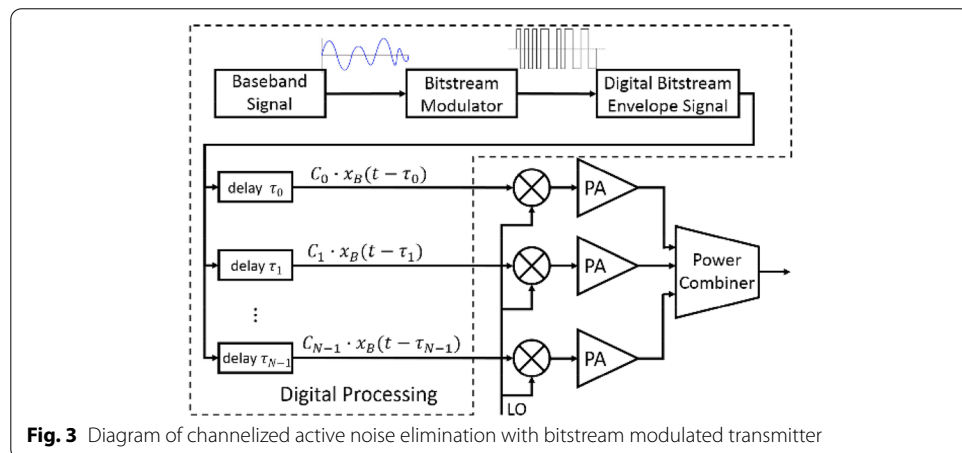
$$h_B(t) = \sum_{k=0}^{N-1} C_k \delta(t - k\tau) \quad (1)$$

$$H_B(f) = \sum_{k=0}^{N-1} C_k e^{-j2\pi k\tau f} \quad (2)$$

Denoting the baseband EDSM signal and its spectrum by $x_B(t)$ and $X_B(f)$ and assuming all the mixer plus PA channels are identical with a large-signal gain A , the up-converted and combined RF signal at the output of the combiner is given by:

$$y(t) = e^{j2\pi f_c t} \sum_{k=0}^{N-1} A C_k x_B(t - k\tau) \quad (3)$$

Whose spectrum is given by:



$$Y(f) = AX_B(f - f_c)H_B(f - f_c) \quad (4)$$

It is thus evident that the CANE filter transfer function $H_{RF}(f)$ is an up-converted version of $H_B(f)$ at the center frequency of f_c , i.e.,

$$H_{RF}(f) = H_B(f - f_c) \quad (5)$$

For instance, in a N-channel uniform combining CANE, let τ denote the delay unit, the filter transfer function is

$$H_{RF}(f) = e^{-j(N-1)\pi(f-f_c)\tau} \frac{\sin(N\pi(f-f_c)\tau)}{\sin(\pi(f-f_c)\tau)} \quad (6)$$

The rejection bands are thus located at:

$$f_{rej} = f_c \pm \frac{M}{N\tau} \quad (7)$$

where M is an integer and $M \neq kN, k = 0, 1, 2, \dots$

The first null-to-null bandwidth of the passband is

$$BW_{null} = \frac{2}{N\tau} \quad (8)$$

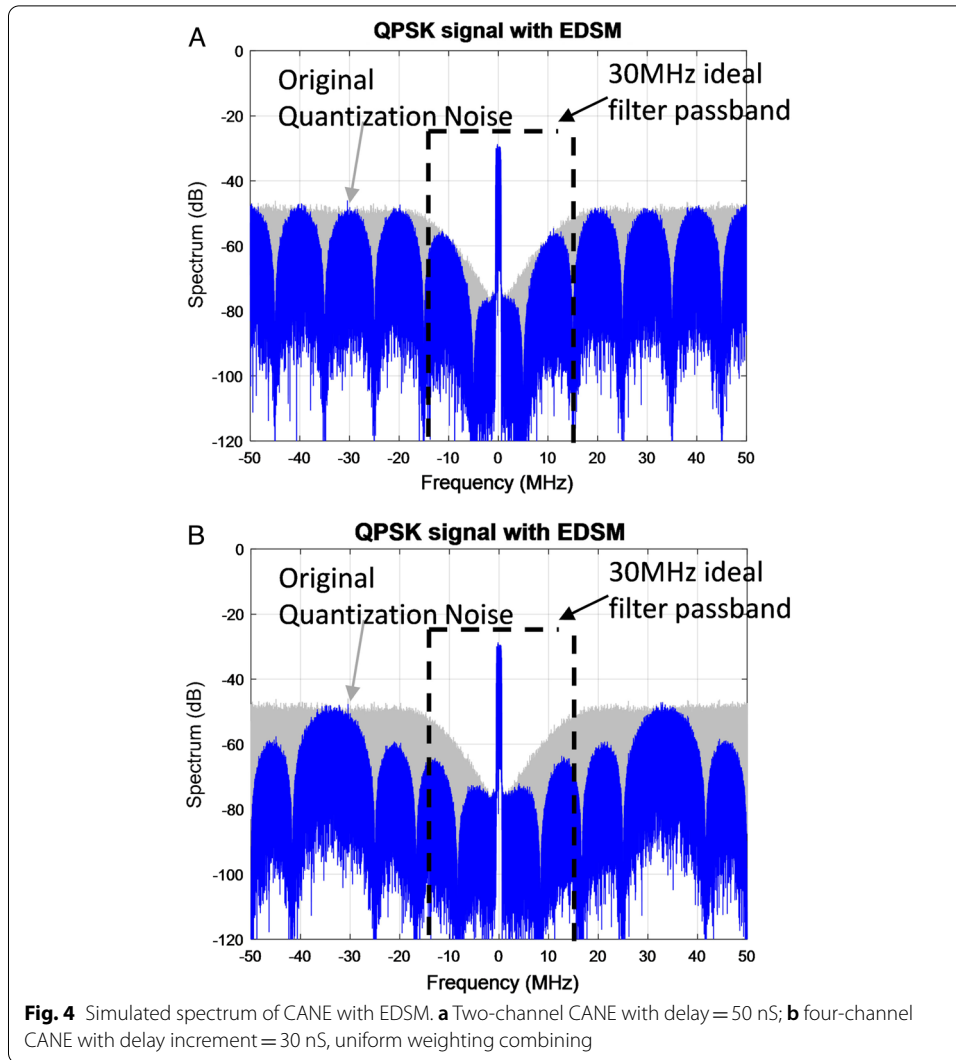
From (7) and (8), all the rejection bands are symmetrically distributed with the center at f_c , while a longer delay unit yields a narrower passband. It is also evident from (5) that the center frequency of the central pass band is solely determined by the LO frequency f_c and irrelevant to the choice of time delay. Therefore, one may change the filter bandwidth by tuning the delay length at baseband without disturbing the center frequency of the RF passband.

Figure 4 displays the simulated spectrum of CANE with EDSM. The testing signal is 1 MHz QPSK signal modulated by 2 level EDSM with a clock rate of 100 MSPS. The spectrum of the original EDSM signal without any noise suppression is plotted as the background in gray for comparison. Figure 4a displays the two-channel CANE with the second channel delayed by 5 clocks, i.e., 50 ns. It is observed that in 4(a), the first pair of nulls appear at $f_{rej} = \pm 10\text{MHz}$ offsets from the center frequency, and thus, the first null to null bandwidth is 20 MHz. Figure 4b displays the spectrum with four-channel CANE combined with a uniform weighting at a delay increment of 30 ns. Compared with Fig. 4a and b, the four-channel case has provided better noise suppression over a wider frequency band.

To quantify the filtering performance of CANE, the signal-to-quantization noise ratio can be employed as a figure of merit. Denoting the complex, baseband spectrum of the bitstream modulated signal by $S_{BMT}(f)$ and signal bandwidth by Sbw , the in-band signal power P_{IBSIG} can be expressed as:

$$P_{IBSIG} = \int_{-Sbw}^{+Sbw} |S_{BMT}(f)|^2 df \quad (9)$$

Note that CANE is often jointly used with an analogue output filter, it is important to evaluate the noise suppression within the analogue filter passband, as shown in Fig. 2. Let FBW be the bandwidth of the analogue filter, the in-band quantization



noise power can thus be calculated by integrating the noise power within the analogue filter passband yet outside the desired signal band, i.e.,

$$P_{QNF} = \int_{-\frac{FBW}{2}}^{-\frac{Sbw}{2}} |S_{BMT}(f)|^2 df + \int_{+\frac{Sbw}{2}}^{+\frac{FBW}{2}} |S_{BMT}(f)|^2 df \quad (10)$$

Therefore, the signal-to-quantization noise ratio subject to the analogue filter is defined as:

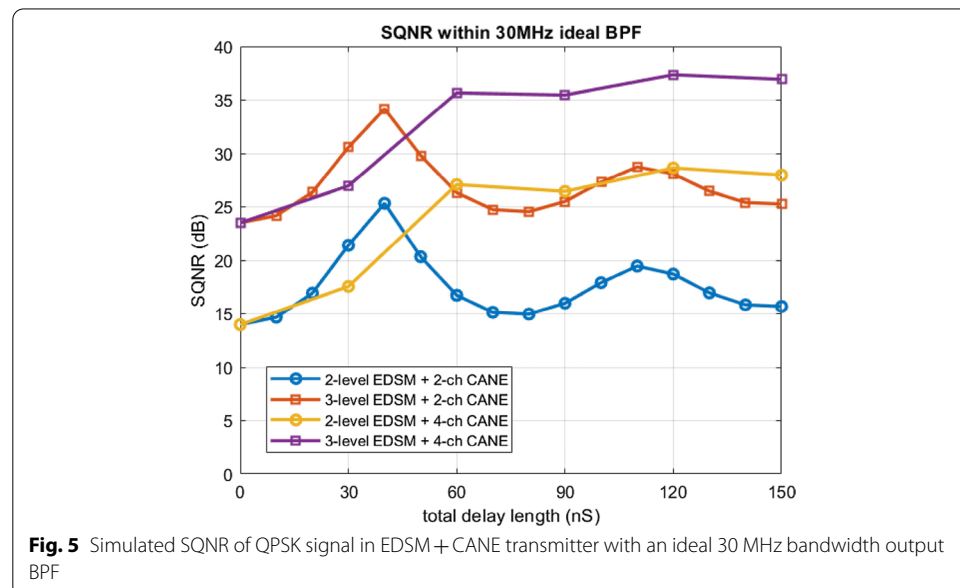
$$SQNR = \frac{\int_{-\frac{Sbw}{2}}^{+\frac{Sbw}{2}} |S_{BMT}(f)|^2 df}{\int_{-\frac{FBW}{2}}^{-\frac{Sbw}{2}} |S_{BMT}(f)|^2 df + \int_{+\frac{Sbw}{2}}^{+\frac{FBW}{2}} |S_{BMT}(f)|^2 df} \quad (11)$$

For example, in the cases shown in Fig. 4a and b, the original EDSM signal has an unfiltered SQNR of 0.96 dB. With the two-channel CANE at 50 ns delay and 100 ns delay, the unfiltered SQNR is increased to 3.75 dB and 3.96 dB, respectively.

In contrast, the original SQNR of EDSM signal within the 30 MHz analogue filter passband is 13.97 dB before CANE is applied. It has been improved to 20.33 dB and 17.9 dB, respectively, with the two-channel CANE at 50 ns and 100 ns delays. When the four-channel CANE with a delay increment of 30 ns is applied, the unfiltered SQNR becomes 7.43 dB. The filtered SQNR becomes 26.44 dB, which is about 12 dB improvement compared to the case without CANE.

It is also important to observe the CANE filter performance incorporating a physical BPF as a function of the delay length, which can help to find the best delay. Figure 5 plots the simulated SQNRs for different configurations with the 30 MHz BPF in place. From the plot, it is evident that CANE with more channels can offer better quantization noise suppression, as the four-channel CANE yields a higher SQNR compared to the two-channel case. The choice of delay may also be optimized for the best quantization noise suppression performance. A longer delay in CANE offers a narrower active filter passband with lower noise in this passband but a second or third digital passband may appear inside the analogue filter band, represented by the grating lobes of the SINC function in (6), while a shorter delay line may push those higher-order passbands outside the analogue filter band but at the price of an increased active filter passband with potentially higher residue noise in the band. In the two-channel case, 40nS delay on the second channel offers the best SQNR. Because the quantization noise from EDSM proportionally increases as frequency offset raises, the 40nS delay case places the digital filter stop band right next to the BPF cutoff frequency, where the noise is strongest.

Typically, higher in-band SQNR indicates that the PA delivers more power to the useful signal other than the noise and may lead to a better effective power efficiency. The in-band signal occupation ρ_{IBSO} can be used to show how much power filled into the desired signal band versus the total power output from the PA module.



$$\rho_{IBSO} = \frac{\int_{-\frac{FBW}{2}}^{+\frac{SBW}{2}} |S_{BMT}(f)|^2 df}{\int_{-\frac{FBW}{2}}^{+\frac{FBW}{2}} |S_{BMT}(f)|^2 df} \times 100\% \quad (12)$$

The overall PA effective efficiency can be defined as the total power in the desired signal band divided by the DC power consumption, which can be equivalently estimated by the production of the PA efficiency and the in-band signal occupation.

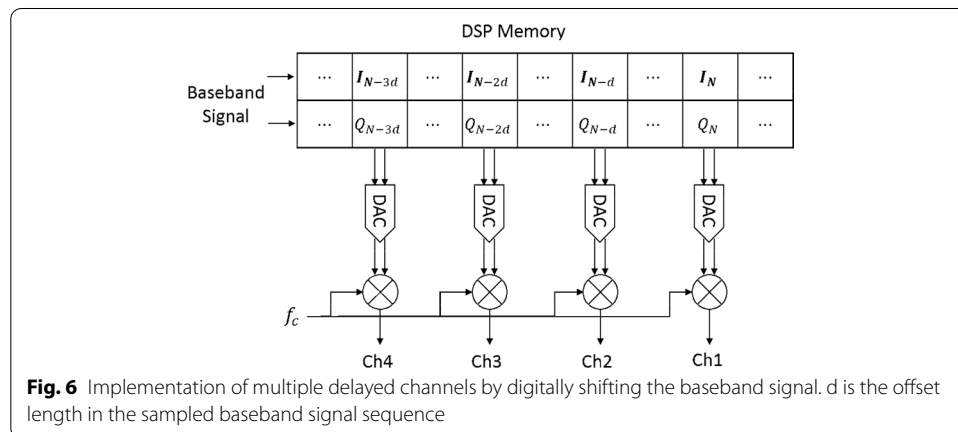
2.2 Digital control and calibration

As shown in Fig. 3, all the delay operations in a CANE transmitter can be implemented by digital signal processing without RF or analogue delay lines. Therefore, CANE filter can be reconfigured in a digital signal processor without physically changing the hardware. Digitally shifting registers that store the I and Q data in a DSP/FPGA processor is a relatively easy and time-efficient task. The resolution of the time delay setting can be as fine as one sampling clock. Since the baseband signal is identical for all the channels, the memory usage can be minimum. Figure 6 shows an example of such data storage/shifting architecture, where the I and Q data are shifted to the next register at each clock and the d th, the $2d$ th so on to the Nd th samples are output to the DACs corresponding to the multiple delayed channels with a time-delay interval of d clocks.

Since the delayed baseband signal is up-converted to RF, there might be phase error among the multiple LOs which will be carried over to the up-converted RF signals. In this system, the phase error generated by in each path mainly behaves as a constant angle offset. The phase error may affect the filtering performance and must be calibrated with a phase control circuitry at each LO path or simply with an arithmetic phase rotation between the I and Q paths at the input of each DAC by applying different weightings to these two data paths. For example, denote RF output signal with the phase and amplitude error in i th channel by

$$\tilde{y}_i(t) = A_{e,i} y_i(t) \cdot e^{j\phi_{e,i}} \quad (13)$$

where $A_{e,i}$ represents the ratio of the non-calibrated amplitude for i th channel and the ideal one. $A_{e,i} = 1$ if there is no amplitude error. $\phi_{e,i}$ represents the phase offset of the i th channel. $y_i(t)$ is the time domain signal output from i th PA path. To mitigate the phase



and amplitude error, one can apply calibration on the baseband input before loading the signal to DAC, for i th channel, the corrected I and Q paths are given by:

$$\tilde{I}_i(t) = \frac{1}{A_{e,i}} (I_i(t) \cos \phi_{e,i} + Q_i(t) \sin \phi_{e,i}) \quad (14)$$

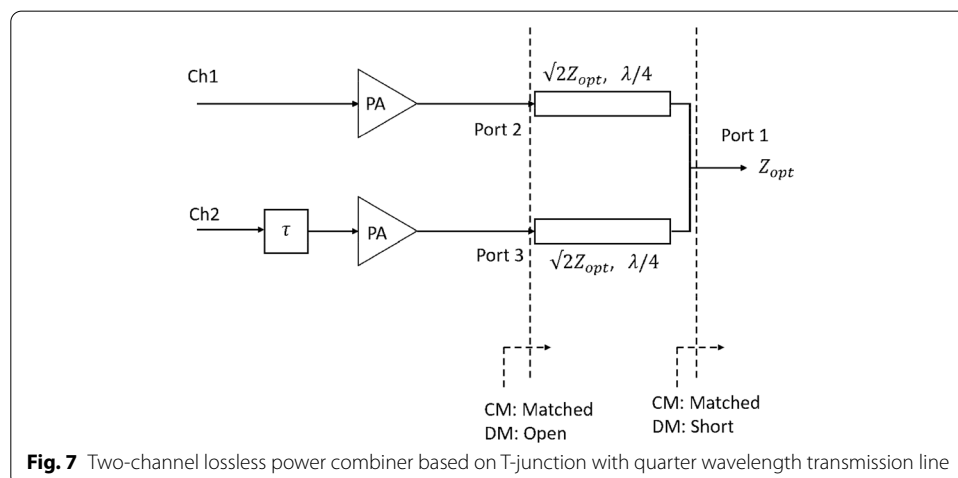
$$\tilde{Q}_i(t) = \frac{1}{A_{e,i}} (I_i(t) \sin \phi_{e,i} - Q_i(t) \cos \phi_{e,i}) \quad (15)$$

The calibration aligns the amplitude and phase of all the in-band signal after up-converting and amplification. The center frequency and the signals are combined in phase with theoretically no insertion loss. The digital calibration waives physical tuning of the RF circuitry, yet providing additional flexibility in RF signal control, such as multi-band EDSM signal generation and noise canceling [12], or fine tune of the center frequency of the passband.

2.3 Power combiner design

After the RF signals with multiple delays are generated, a power combiner is used to combine the signals that are in-phase, i.e., in band, and reject those are out-of-phase, i.e., out of band. The suppression of out-of-band quantization noise can be accomplished in an absorptive fashion with a Wilkinson power combiner or in a reflective manner with a lossless power combiner. In a BMT, the power of quantization noise is a significant portion of that is being amplified. It must be reflected back to the power supply in order to maintain the high power efficiency. In the PLM PA [7], the recycling of the quantization noise power is achieved by utilizing a switching mode power amplifier with voltage source type output terminated by a current-rejection filter. The out-of-band signal at the PA thus sees a high impedance load which reflects its power back to the supply without causing dissipation. Similar strategies can be employed in CANE by properly designing the power combiner to exhibit a high impedance load to the out-of-phase or out-of-band signal, yet presenting the optimum load for in-phase or in-band signal.

For example, Fig. 7 shows a plot of the two PAs combined by a T-junction-based power combiner. For in-band signals, the two paths are delivering identical signals in



a common mode while the out-of-band signals are combined anti-phase which follows a difference mode. The S-parameter of the two-way combiner is:

$$[S] = \begin{bmatrix} 0 & -\frac{j}{\sqrt{2}} & -\frac{j}{\sqrt{2}} \\ -\frac{j}{\sqrt{2}} & \frac{1}{2} & -\frac{1}{2} \\ -\frac{j}{\sqrt{2}} & -\frac{1}{2} & \frac{1}{2} \end{bmatrix} \quad (16)$$

Port 1 is the output of the combiner, while port 2 and port 3 are connected to the output of two PAs. Assume the output is terminated by the optimum load and the two PA outputs have a phase difference due to delays, the incoming signal flowing into the three-port combiner network can be written as:

$$[V^+] = [0, V_0, V_0 e^{-j2\pi\tau\Delta f}]^T \quad (17)$$

where τ is the baseband time delay on the second channel, and Δf refers to the frequency offset from the center. Note that the PLM PA is operating in the form of a switched voltage source, the incidence to the three-port combiner is thus represented by the voltages shown in Eq. (17). For the in-band signal, Δf is approximately zero; thus,

$$[V^+]_{inband} = [0, V_0, V_0]^T \quad (18)$$

The outgoing waves are given by:

$$[V^-]_{inband} = [S][V^+]_{inband} = [-j\sqrt{2}V_0, 0, 0]^T \quad (19)$$

This means that the PAs are terminated by the optimum matched load and their output is combined without loss.

For the out-of-band (OOB) signal, the outgoing wave is:

$$V_{1,OOB}^- = -\frac{j}{\sqrt{2}} V_0 (1 + e^{-j2\pi\tau\Delta f}) \quad (20)$$

$$V_{2,OOB}^- = \frac{1}{2} V_0 (1 - e^{-j2\pi\tau\Delta f}) \quad (21)$$

$$V_{3,OOB}^- = \frac{1}{2} V_0 (-1 + e^{-j2\pi\tau\Delta f}) \quad (22)$$

Equation (20) reveals that when the two PAs are out of phase, the output power exhibits a periodically filtered pattern as shown in Fig. 8a.

In the rejection band, especially at the nulls of the filter, where the offset frequency satisfies the condition (7), two channels are out of phase by 180 degrees which forms a differential mode. An equivalent short circuit is formed at the combining junction which is later transferred to open circuit by the quarter wavelength transmission line looking out from the output of each PA. Denoting the input as $[V^+]_{rej} = [0, V_0, -V_0]^T$, the outgoing signals are obtained as,

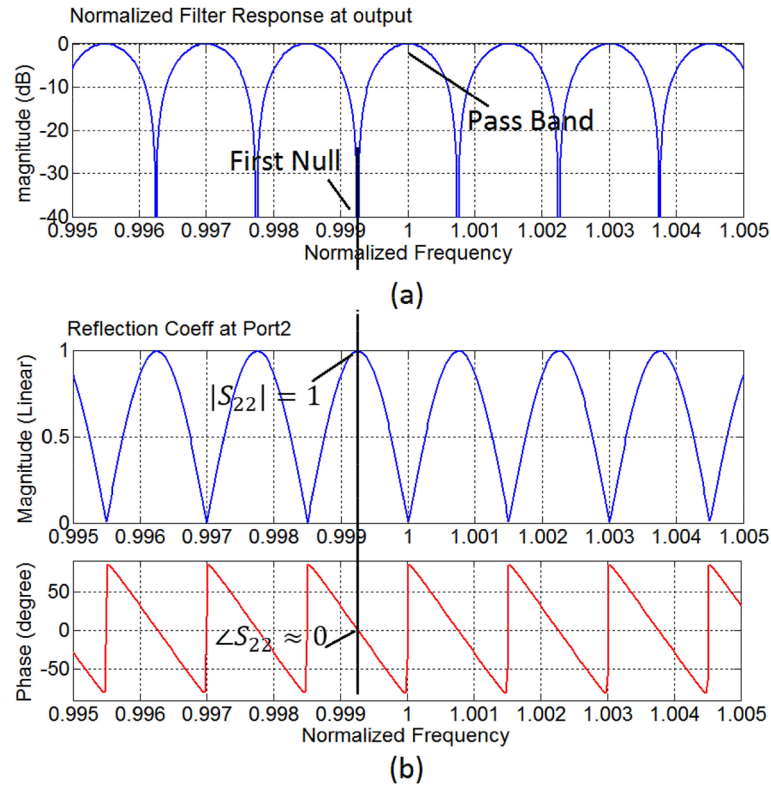


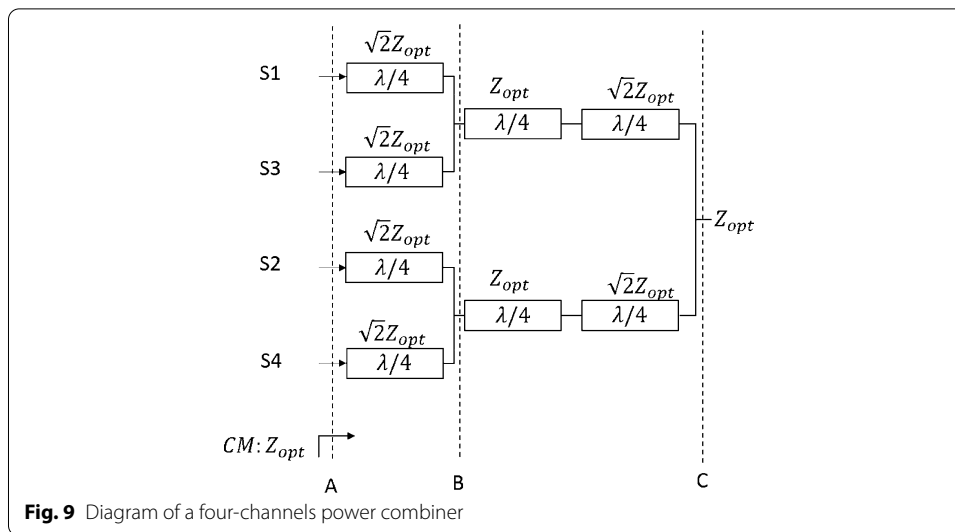
Fig. 8 Simulated filter response of the two-channel power combiner versus frequency. **a** The normalized filter transfer function. **b** The magnitude and phase of the reflection coefficient at one input port

$$[V^-]_{rej} = [S][V^+]_{rej} = [0, V_0, -V_0] \quad (23)$$

This proves that the two input ports now exhibit open-circuit impedance for the differential mode. The input impedance of the combiner versus frequency is derived by simulating the phase and magnitude of the reflection coefficient at one of the input ports, which is plotted against the filter transfer function in Fig. 8b. At the center frequency, the filter transfer function has a magnitude about 1 that indicates all the signal power is delivered to the load. In the filter rejection band, the equivalent reflection coefficient at port 2 and port 3 is:

$$\Gamma_2 = \Gamma_3 = 1 \quad (24)$$

This indicates that the output of each PA at this frequency is indeed completely reflected by the open circuit. The same principle can be utilized to design power combiners for more channels. Figure 9 shows a design of four-channel power combiner. One may prove that the load impedance of Z_{opt} is transformed to Z_{opt} at each of the 4 input ports (reference plane A) in common mode. The input impedance is open circuit for difference modes between any of the two branches, as short circuit is formed either in reference plane B or plane C.



2.4 Bandwidth consideration

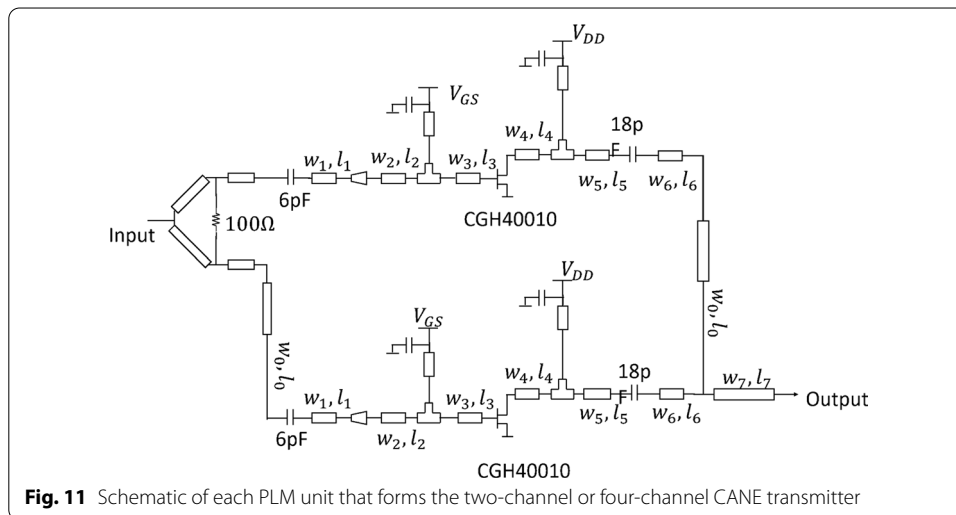
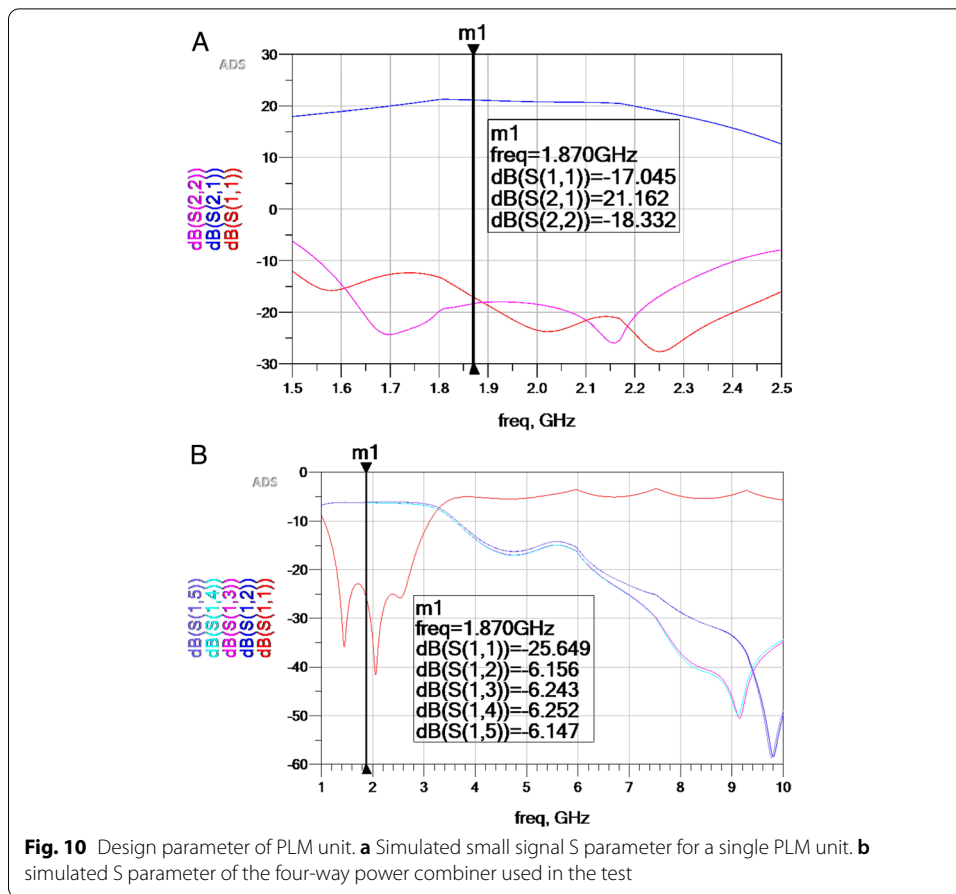
The bitstream modulated transmitter includes baseband sampling, RF amplification and filtering. Each part in the signal path may affect the system bandwidth. In this work, the RF components are designed to offer sufficient bandwidth. The PLM PA units operate from 1.8 to 2.1 GHz. The four-way combiner including multi-section transmission line-based impedance transformers is with a wide bandwidth as shown in Fig. 10. The bandwidth limitation relevant to the proposed transmitter is twofold. The first is the limited bandwidth of the bitstream modulation generator. The clock rate of EDSM needs to be much higher (8 to 10 times greater) than the envelop bandwidth to shape the quantization noise away from the signal band. It is also desired that the sampled waveform to be rectangular pulse trains with fast rising and falling edges. This further elevates the desired sampling rate in a digital implementation. The second bandwidth limitation is limited by the sampling rate of CANE processor which is limited by the technology of the controller implementation (DSP, FPGA or ASIC). The maximum sampling rate of the current FPGA CANE processor is 100MSPS which limits the signal bandwidth to be less than 50 MHz.

In the current setup, the EDSM generator bandwidth limit is dominant. While various envelope modulation techniques [8,22,-24] or a mixed signal EDSM generator implementation could be used to further reduce the noise level and the required sampling rate, we choose 1.2 MHz QPSK signal with 5.3 dB PAPR and 1.4 MHz LTE signal with 10 dB PAPR to demonstrate the proposed concept. Future work will consider higher sampling rate platform and different envelope modulation technique.

3 Experiment

3.1 Power amplifier design

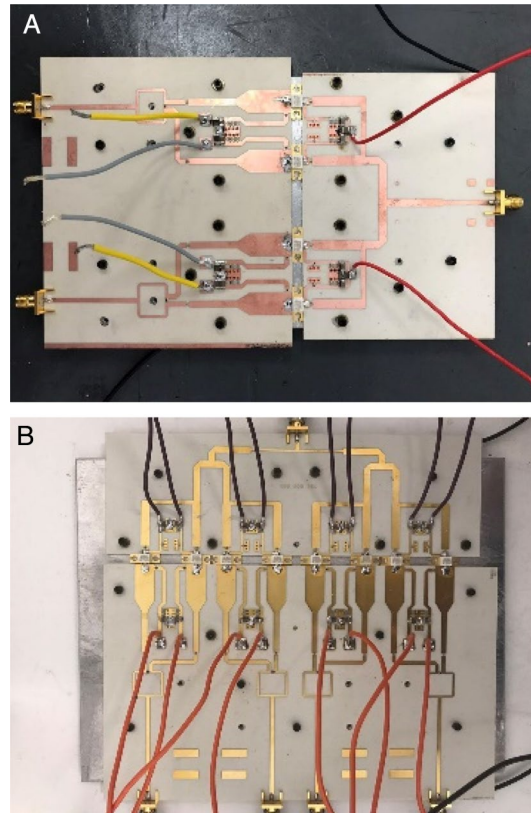
To verify the proposed concept, we fabricated two BMTs at the frequency of 1.8–2.1 GHz for demonstration of two-channel and four-channel CANE. The two-channel transmitter has two sets of PLM PAs where each consists of two Wolfsped



CGH40010 GaN transistors that are connected with a quarter wave length transmission line in between [7] (Fig. 11). The dimensions of the transmission line shown in the diagram are listed in Table 1.

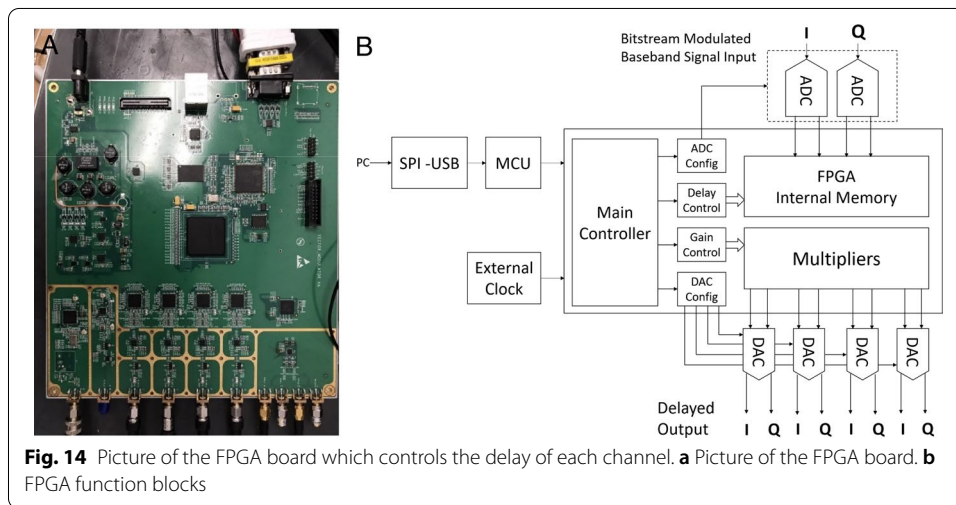
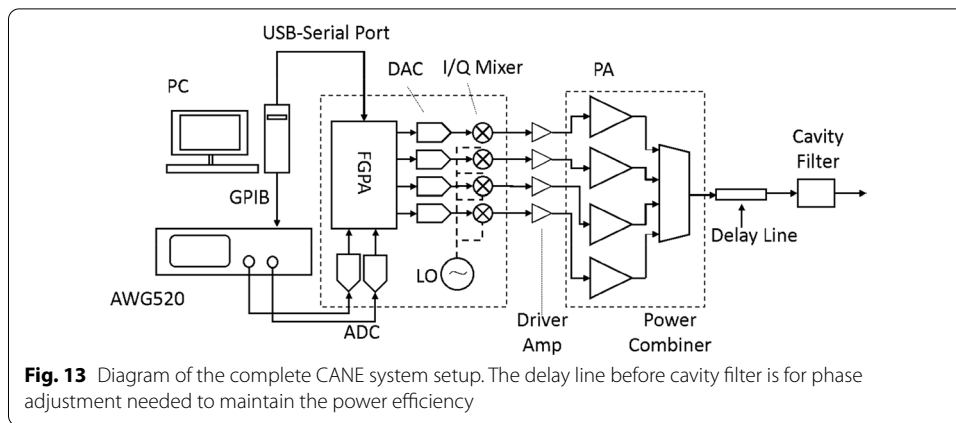
Table 1 Dimensions in the PLM Unit

$w_0 = 70 \text{ mil}$	$w_1 = 100 \text{ mil}$	$w_2 = 350 \text{ mil}$	$w_3 = 350 \text{ mil}$
$l_0 = 800 \text{ mil}$	$l_1 = 750 \text{ mil}$	$l_2 = 550 \text{ mil}$	$l_3 = 40 \text{ mil}$
$w_4 = 100 \text{ mil}$	$w_5 = 100 \text{ mil}$	$w_6 = 100 \text{ mil}$	$w_7 = 120 \text{ mil}$
$l_4 = 20 \text{ mil}$	$l_5 = 20 \text{ mil}$	$l_6 = 760 \text{ mil}$	$l_7 = 800 \text{ mil}$

**Fig. 12** Pictures of power combining modules for CANE. **a** Two-channel CANE. **b** Four-channel CANE

The drain voltage supply is 28 V. At the junction where the main PA and auxiliary PA combine in each of the PLM unit, the optimum output load impedance is designed to be $Z_{\text{opt}} = 25\Omega$. A Chirex power combiner as shown in Fig. 6 is used to combine the two PLM channels. The impedance of the quarter wavelength lines between the PA output and the combiner point is $\sqrt{2}Z_{\text{opt}} = 35.4\Omega$. On the right hand side of the combining point, another 35.4Ω quarter wavelength line is used to match the output impedance to 50Ω . The complete module is terminated with a cavity filter with 30 MHz bandwidth centered at 1.995 GHz. Between the cavity filter and the combiner, a certain length of 50Ω line is employed to create open-circuit termination to the PA at the cavity filter stopband [7].

The designs are further extended to four-channel with a four-channel combiner shown in Fig. 9. A cavity filter with 30 MHz bandwidth centered at 1.87 GHz is used



this time for four-channel test. Pictures of both experimental setups are displayed in Fig. 12a and b.

3.2 Digital system setup

The digital system setup is shown in Fig. 13. The envelope delta-sigma modulation of the complex baseband signal is generated in a personal computer with an EDSM MATLAB code. It is then transferred to a Tektronix arbitrary waveform generator AWG520 through a GPIB port. Control of the delays needed for CANE is realized digitally with a custom developed FPGA board, as shown in Fig. 14a. The board supports 8 parallel channels of A/D sampling, delaying and D/A outputs in real time with a maximum clock rate of 100MSPS.

The function blocks of the FPGA are shown in Fig. 14b. The FPGA is programmed by Verilog and is controlled by a PC through USB-SPI interface. A microcontroller (STM-32F407ZG) which builds a SPI interface that transfers the serial commands from PC to parallel control signals for FPGA. The main controller block in FPGA configures the one dual channel ADC (AD9652) chip and the four DACs (AD9122) chip. One external 100 MHz clock is fed into the FPGA and then being distributed to the other module.

The delay controller reads the FPGA internal memory using the method shown in Fig. 6. The gain controller adjusts the amplitude balance and calibrate the phase derivations between all the DAC outputs. The FPGA used in the test is Cyclone III EP3C120F780I7, which has 532 pins, 120 K logic elements and 576 embedded multipliers and 4 PLLs. However, it is important to mention that this module is only designed for conceptual demonstration, which, however, require only few computational resources on the powerful FPGA. The usage of the FPGA resources is listed in Table 2. In practical use, a simple application-specific integrated circuit (ASIC) chip is preferred for low cost implementation. The program allows a maximum delay of 100uS, or 10 K points under maximum sampling rate of 100MSPS. The FPGA memory only serves as a data buffer for delay operation; therefore, the actual used internal memory of FPGA is about 80KByte with both I and Q data are stored in 32bit format.

The delay operation is conducted by reading the FPGA memory data at an offset address to the D/A converters. The delay resolution is 10 ns due to the maximum clock rate. The delayed complex baseband signals at the outputs of the four pairs of DACs are sent to an IQ mixers and up-converted to the original carrier. Besides generating the required delay in each channel, the RF signal amplitude, carrier frequency and phase offset are also controlled by the FPGA board. The LO is generated on the FPGA board and distributed to the four up-converters. The LO phase deviations between the channels can be calibrated directly from PC by pre-shifting the phases of the baseband signal.

The four-channel RF signals are pre-amplified by four identical driver amplifiers with the part number TQP9111 and fed into the PA modules. The output power and spectrum are measured simultaneously.

4 Results and discussion

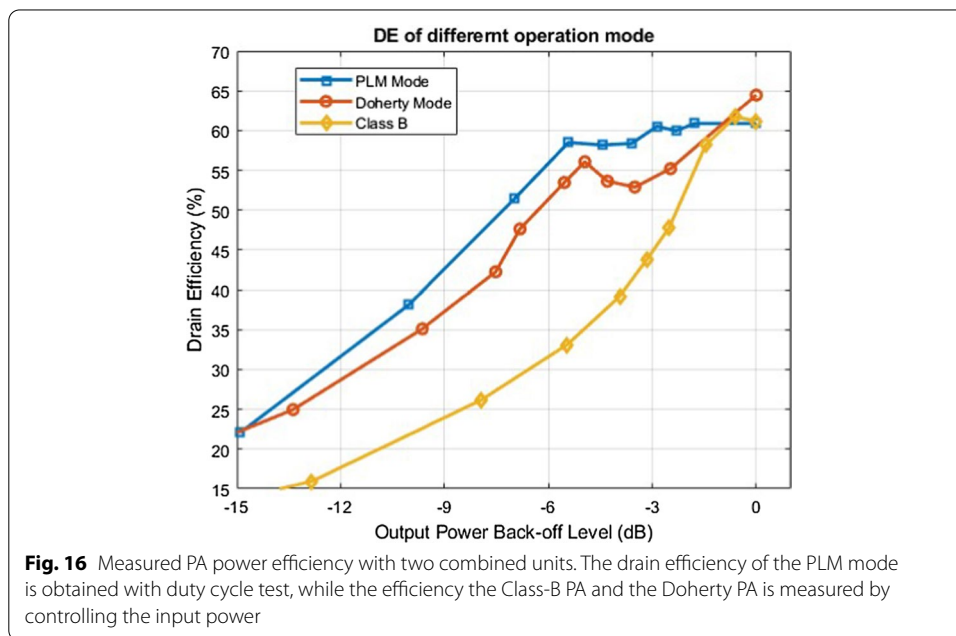
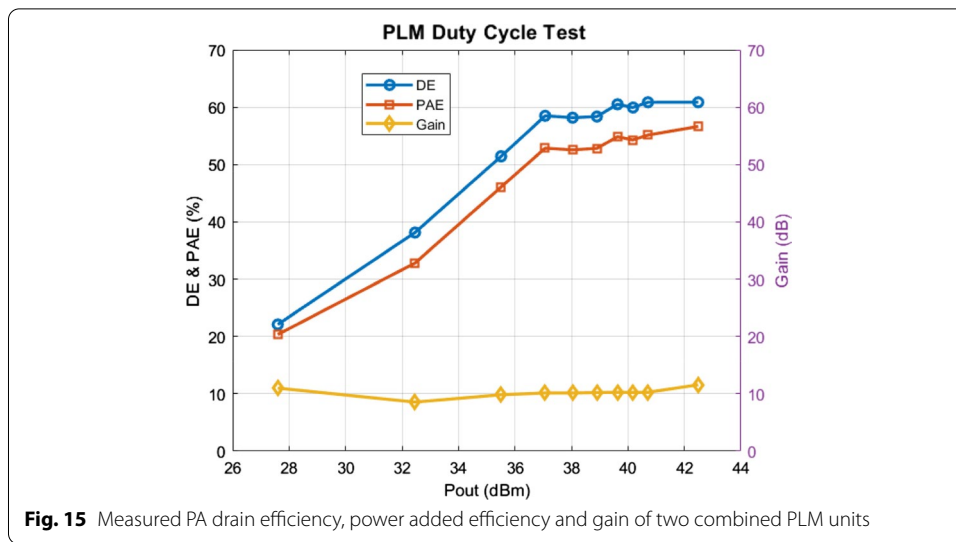
4.1 Results

4.1.1 Measured PLM unit performance

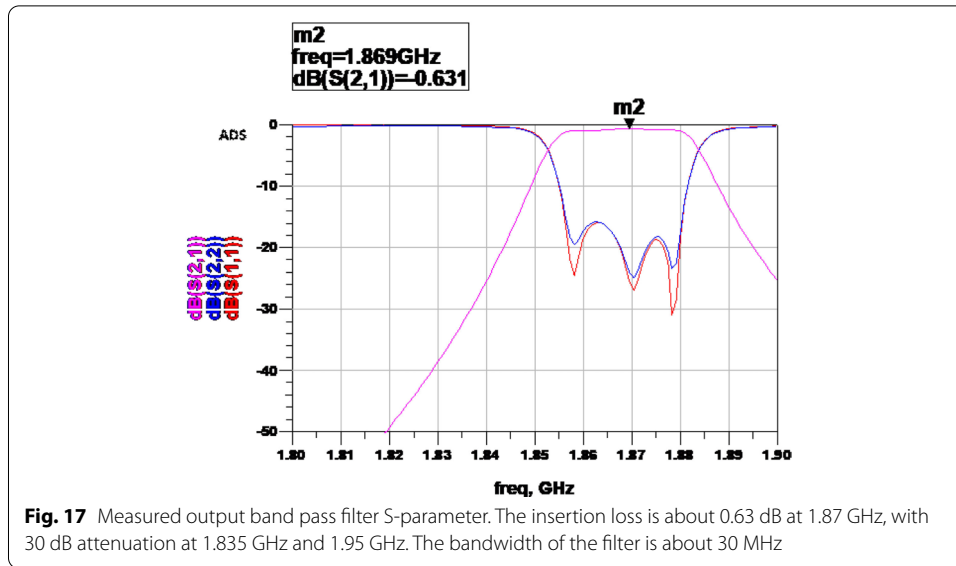
The power performance of the PLM PA unit is first characterized experimentally. The operation frequency of the PLM is designed to be 1.805 GHz to 2.1 GHz. At 1.87 GHz, when the transistors are operating in a balanced class-AB mode, the small signal gain is about 21 dB. To fully explore the switched-mode efficiency performance, we biased both main and auxiliary PAs deeper close to Class B when operating in PLM mode. At 1.87 GHz, the measured drain efficiency, power added efficiency and gain of the PA with two combined units versus output power are shown in Fig. 15. The maximum output power is now 42.5 dBm, and the gain at the saturation point is 11.8 dB

Table 2 FPGA Usage Summary

Resources		Number of used	Total number available	Usage (%)
Logic element	Total	14,805	119,088	12
	Combinational functions	6412	119,088	5
	Dedicated logic registers	13,064	119,088	11
Multipliers		48	576	8
PLL		1	4	25



(Fig. 16). A single PLM unit can output a maximum output power of 39.5 dBm with a maximum drain efficiency of 67% when the 0.63 dB insertion loss of the output cavity filter is de-embedded. The measured S parameter of the filter is also shown in Fig. 17. In the proposed PLM design, the load impedance present at the transistor drain point is selected to maximize the drain efficiency instead of output power. The peak power efficiency is still above 60%, with the loss from the output filter included in the efficiency calculation. The efficiency of the PLM PA is measured with duty cycle control [7] at a pulse repetition rate of 100 MHz. This is compared to the measured result for the same PA operating in conventional class-B mode under input power control in Fig. 13. From the comparison, it is evident that the PLM mode can achieve a flat



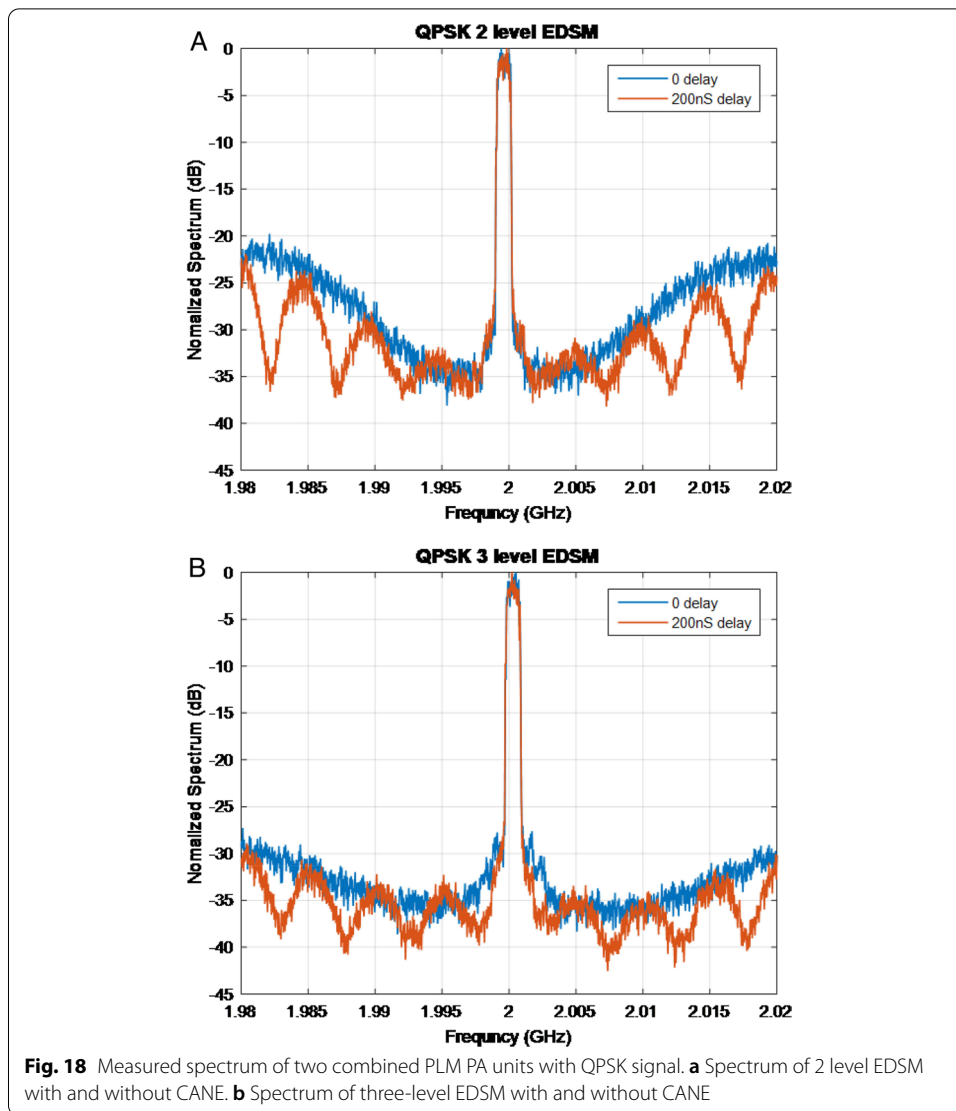
optimal power efficiency curve for power back-off up to 6 dB as predicted by theory [7].

4.2 CANE performance measurement

In the experiment, we tested both two-channel and four-channel CANE with both QPSK and LTE signals. The symbol rate of the QPSK signal has a symbol rate of 1 MSps and is filtered by a square root raised cosine filter with a roll-off factor of 0.2, resulting an occupied bandwidth of 1.2 MHz at 5.3 dB PAPR. The LTE signal under test has a bandwidth of 1.4 MHz and PAPR of 10 dB. This is to test the performance of CANE under a high PAPR condition. The sampling rate of the signal generation is chosen to be 100 MSps to match the sampling speed of the ADC on the FPGA control board. Both two-level and three-level EDSM [10, 11] are used for bitstream modulation. Considering the frequency range adjacent to the desired signal band, the in-band signal linearity within 5 MHz offset adjacent to the center frequency is preserved by the noise shaping function of EDSM and the measured ACLR is about 32–33 dBc for QPSK signal and 29 to 30 dBc for LTE signal, limited by both software code and the amplitude and phase error of the AWG. In general, the three-level EDSM produces less quantization noise than the two-level case, as shown in the plot. In the QPSK test, at 20 MHz offset, the noise in two-level EDSM is about 22 dBc below the in-band signal, while the three-level EDSM has noise level of about 30 dBc. In the LTE test, at 20 MHz offset point, the noise in two-level EDSM is about 18 dBc below the in-band signal, while the three-level EDSM has a noise level of about 23 dBc, which are generally higher than the QPSK cases due to the higher PAPR. Both cases are shown in the background of Figs. 14 and 15.

4.3 Two-channel CANE

For two-channel CANE, the delay length is selected to be 200 nS, which places the first pair of nulls at ± 2.5 MHz offset from the center frequency. The measured output spectrum of the two-channel combining module with QPSK and LTE signal is shown in



Figs. 18 and 19, respectively. The SQNR within the analogue filter passband with and without CANE is calculated from the measured spectrum and listed in Table 3. For QPSK signal with two-level EDSM, CANE improves the SQNR from 7.13 to 10.53 dB which corresponds to in-band signal occupation from 83.81 to 91.87%. For the three-level EDSM test, the measured SQNR with and without CANE is 13.45 dB and 16.52 dB, respectively.

The output power of the PA for two-level EDSM QPSK case is 37.94 dBm and the achieved overall efficiency is 53.8% without CANE. With two-channel CANE, the output power and efficiency become 37.6 dBm and 52.1%, which remain at the same level as the case without CANE. The effective power efficiency, which is defined as the signal power in the defined signal bandwidth versus the total consumed power, may still be higher. The effective efficiency is obtained by multiplying the overall efficiency and the in-band signal occupation ratio, which are 45.1% and 47.8%, respectively, before and after CANE. This indicates that the quantization noise is indeed rejected in a power saving mode. In

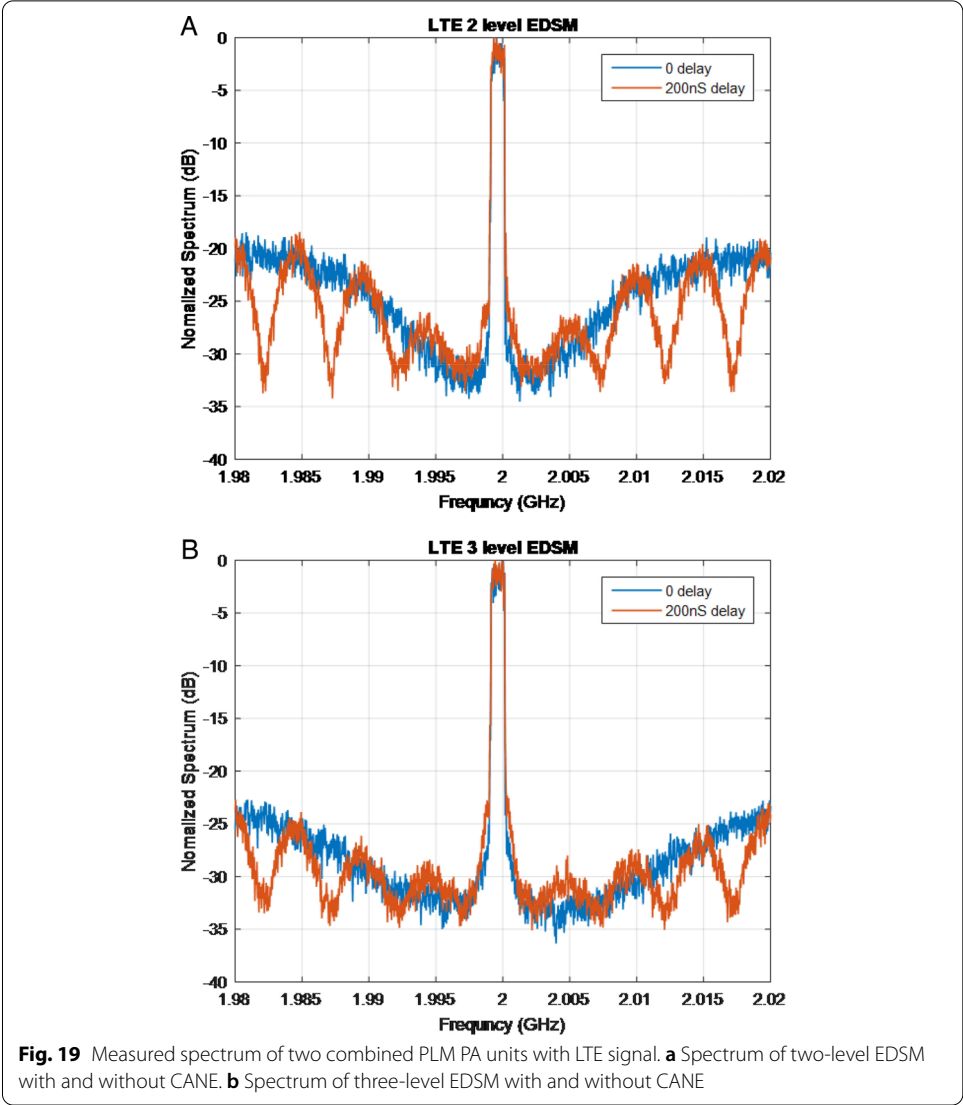


Table 3 Output Power and Drain Efficiency (DE) of Two PAs Combining module

EDSM level	Noise suppression	Pout (dBm)	Efficiency (%)	SQNR (dB)	In-band occupation ρ_{IBSO} (%)
QPSK signal with PAPR of 5.3 dB					
2 level	BPF	37.94	53.8	7.13	83.81
2 level	2 ch CANE + BPF	37.6	52.1	10.53	91.87
3 level	BPF	39.53	59.9	13.45	95.68
3 level	2 ch CANE + BPF	39.38	60.4	16.52	97.82
LTE signal with PAPR of 10 dB					
2 level	BPF	35.95	53.24	4.37	73.24
2 level	2 ch CANE + BPF	35.77	49.75	6.49	81.66
3 level	BPF	36.69	51.92	8.52	87.66
3 level	2 ch CANE + BPF	35.64	49.95	10.58	91.96

the three-level EDSM test with QPSK, the output power increases to 39.53 dBm without CANE and 39.38 dBm with CANE. The power efficiency also increases to about 60%. It is expected that the multi-level EDSM improves both the output power and efficiency as less of the in-band power is attributed to quantization while more of that power is corresponding to the desired signal, yet minor improvement of effective power efficiency from 59.9 to 60.4% is observed.

Similar improvement of SQNR can be seen in the LTE test. The SQNR improvement in two-level and three-level EDSM cases is 2.12 dB and 2.06 dB, respectively, while the effective efficiency remains about 50%.

4.4 Four-channel CANE

It is evident that a higher PAPR signal such as LTE signal tends to generate a higher quantization noise which may require a multi-channel CANE for deeper noise suppression. The four-channel CANE is tested with LTE signal for such purposes. Three cases including a non-delayed case, a two-channel case and a four-channel uniform combining case are tested and compared with the measured spectrum as shown in Fig. 16. The two-channel test is implemented by setting two of the total four channels with zero delay and the other two with 100 nS delay. The delay unit in the four-channel test is 30 nS, which corresponds to delay lengths of 0 nS, 30 nS, 60 nS and 90 nS, respectively.

In the spectrum of the two-channel case shown in Fig. 20, the nulls appear at 5 MHz offset from the center frequency at first, then every 10 MHz offset from the first nulls. However, at some frequencies the quantization noise is not well suppressed due to the appearance of second passbands in between stopbands. These second passbands can be further suppressed to form a wider stopband with the four-channel uniform combining scheme as shown in the red curve in Fig. 20.

Table 4 lists the measured power, efficiencies and linearity performance. The SQNR and in-band signal occupation are also calculated from the measured data for each case. For the two-level EDSM, the two-channel CANE improves the SQNR by 3.17 dB, while the four-channel improves it by 10.93 dB. For the three-level EDSM, the two-channel CANE increases SQNR by 2.7 dB, while the four-channel CANE improves it by 5.33 dB. The output power and efficiency remain at the same level, while the effective efficiency has increased from 41.41% in the non-delay case to 46.06% in the two-channel case and 48.14% in the four-channel case. Similar trend is observed in the three-level EDSM case, while the power efficiency is slightly lower due to the fact three-level EDSM traded power efficiency for better SQNR. Considering the amplifier has 11.8 dB gain when driven in PLM mode, the three-level EDSM LTE signal with four-channel CANE has achieved a PAE of 43.6%

4.5 Discussion

4.5.1 Discussion of measured results

The measured ACLR curve shows that CANE technique can effectively suppress undesired out-of-band noise, especially at the nulls of the filter. In Fig. 21a, the blue curve shows the noise suppression only by the BPF. As the frequency offset goes further, ACLR becomes worse due to the noise shaping by EDSM. With two-channel CANE, the ACLR is improved until the 4th adjacent channel and starts to drop, because the

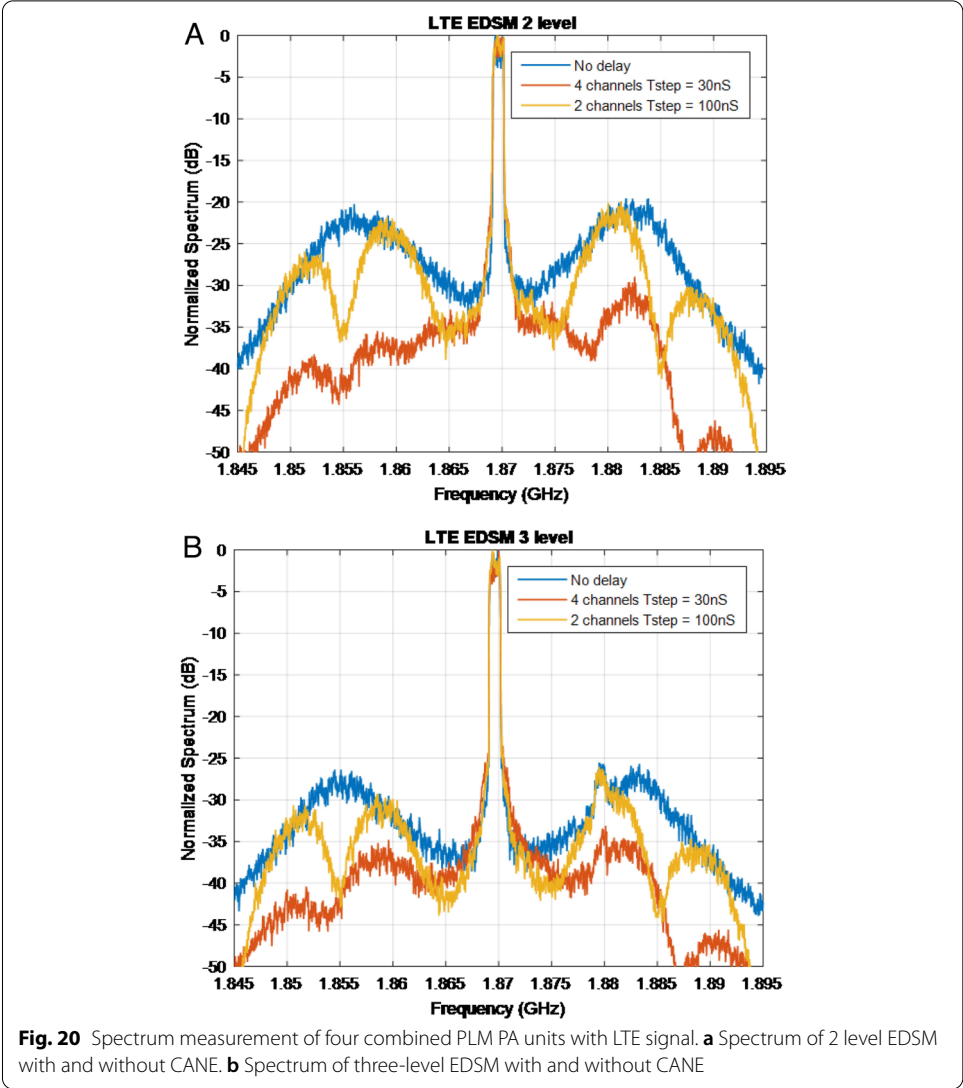
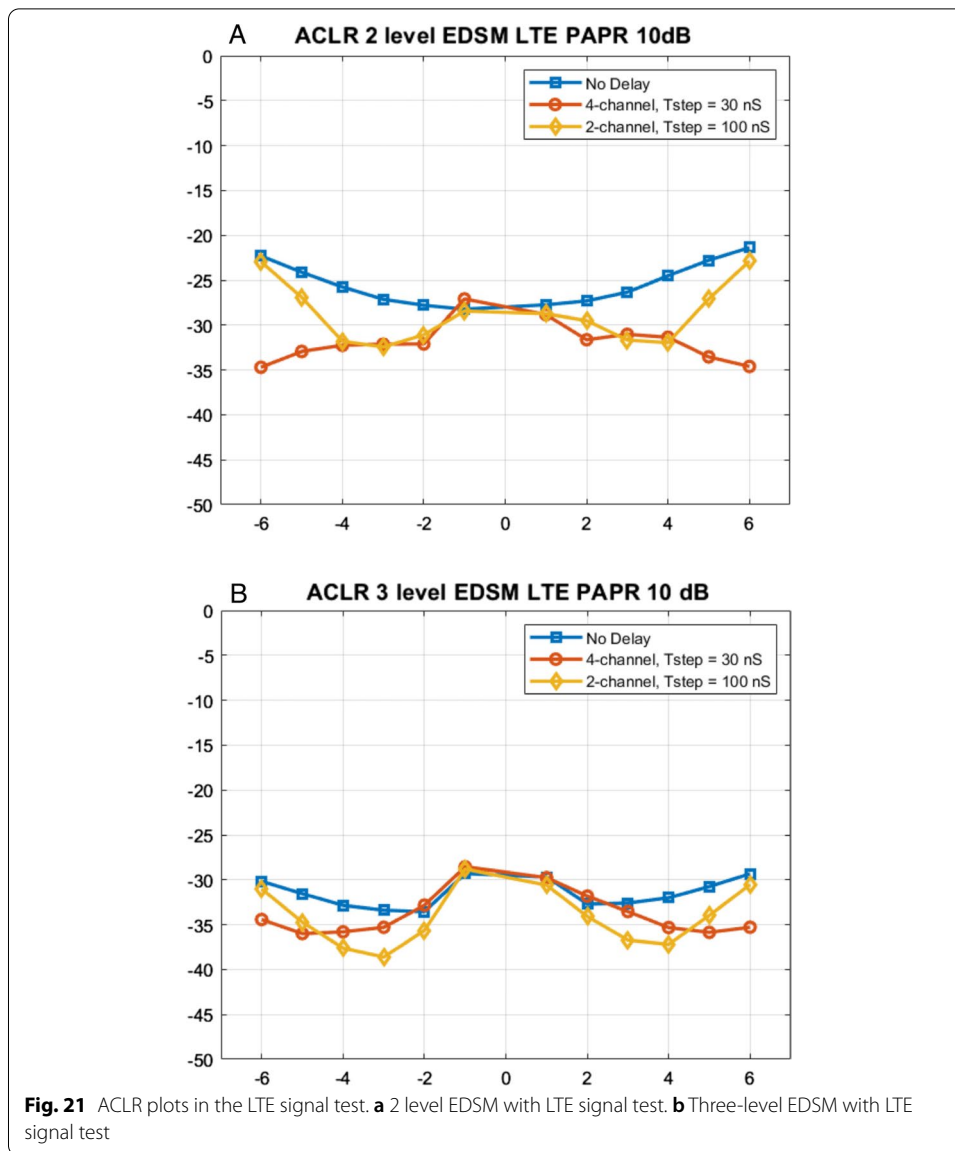


Table 4 Output power and drain efficiency (DE) of four PAs combining module

EDSM level	Noise suppression	Pout (dBm)	Efficiency	SQNR (dB)	In-band occupation <i>ρ_{IBSO}</i>
LTE signal with PAPR of 10 dB					
2 level	BPF	40.1	49.38%	7.16	83.86%
2 level	2 ch CANE + BPF	40.82	50.33%	10.33	91.52%
2 level	4 ch CANE + BPF	40.98	48.88%	18.09	98.48%
3 level	BPF	41.25	46.78%	13.32	95.56%
3 level	2 ch CANE + BPF	42.18	47.19%	16.02	97.56%
3 level	4 ch CANE + BPF	41.67	46.42%	18.65	98.66%

second passband of the digital filter falls into the BPF passband. With four-channel noise suppression, the ACLR is gradually improved along with the channel offset, because the four-channel filter offers wider rejection band which can sufficiently eliminate the

**Table 5** PERFORMANCE comparison

	Signal PAPR	Frequency	technique	Pout	Efficiency	ACLR	ACLR wDPD
This work	1.4 MHz LTE/10 dB	1.87 GHz	EDSM + CANE	41.67 dBm	DE 46.2% PAE 43.6%	-29dBc/- 30dBc	No DPD
[22]	10 MHz LTE/7 dB	2.35 GHz	EDSM	25.5 dBm	DE 48%	-31dBc/- 32dBc	—
[6]	5 MHz LTE/6 dB	700 MHz	DSM	24.7 dBm	DE 56%	-39 dBc	-45.1 dBc
[25]	10 MHz LTE/7.5 dB	1.6–2.1 GHz	Doherty	27.5 dBm	PAE 36%	-32 dBc	No DPD
[26]	WCDMA	2.14 GHz	Doherty	35.3 dBm	PAE 39.6	-25.3 dBc	—
[27]	DL-WiMax / 9 dB	2.14 GHz	Digital Doherty	36.8 dBm	DE 50%	-25dBc/-	-46 dBc

quantization noise. In addition, the three-level EDSM case can provide overall better noise rejection as the quantization noise is intrinsically lower. Table 5 compares the performance of this work and other techniques, particularly those with Doherty techniques. It can be seen from the table that the proposed transmitter is better than conventional Doherty amplifiers in power efficiency. Its linearity is also better than Doherty before DPD; however, it falls short on the linearity in comparison with the Doherty+DPD approach.

The ACLR performance of the current BMT is limited by both the modulation non-idealities and the quantization noise. To overcome modulation non-idealities, a better digital modulator [6, 20] with shorter rise and fall times could be implemented. For further quantization noise suppression, a number of parallel units such as that in a phased array can improve the linearity performance significantly.

4.5.2 Computational complexity comparison

The digital architecture used for CANE is significantly simpler than that of DPD. In DPD, the DSP needs to calculate the power series of the input at high speed (three to five times faster than the signal bandwidth to allow modeling of the higher-order terms). It thus involves a great amount of real-time multiplication operations. CANE only involves with digital delays of the input with constant weighting coefficients that are preset. The weighting coefficients are coefficients of the digital FIR filter. In fact, only uniform weighting is used in the manuscript.

It should also be noted that the digital delay lines as implemented are over designed for general purposes. For small bandwidth baseband signal, it can be significantly simplified by cascading multiple digital delay lines that offer a binary combination of delays and driven by different clocks. The lowest clock frequency just needs to be higher than the Nyquist rate and the highest clock frequency can offer a fine delay resolution. In this case, only a few shift registers are needed and only one shift register needs to be driven at the highest clock frequency, which will yield a high delay resolution yet with small chip area and low power consumption.

5 Conclusion

The paper presents the technique of CANE including the fundamental theory, simulation results, hardware implementations and experimental results. The technique is applied to a combination of multiple high efficiency GaN power amplifiers. These amplifiers are designed for bitstream modulations with pulsed load modulation technique applied to achieve high power efficiency during power back-off. CANE is applied to suppress the quantization noise yet to maintain its high power efficiency under different types of modulations based on a lossless power combining architecture. A two-channel and four-channel CANE testbed is setup and tested. The experimental results have proven that CANE can serve as a digitally reconfigured active filter directly at the RF output of a bitstream modulated transmitter. The proposed technique provides an effective quantization noise reduction technique that is complementary to conventional passive filters without compromising the system power efficiency.

Abbreviations

RF: Radio frequency; FIR: Finite impulse response; PAPR: Peak-to-average power ratio; ET: Envelope tracking; DPD: Digital pre-distortion; BMT: Bitstream modulated transmitter; PWM: Pulse width modulation; EDSM: Envelope delta-sigma modulation; PLM: Pulsed load modulation; ACLR: Adjacent channel leakage ratio; PA: Power amplifier; CANE: Channelized active noise elimination; FPGA: Field programmable gate arrays; ASIC: Application-specific integrated circuit; LO: Local oscillator; SQNR: Signal-to-quantization noise ratio; DSP: Digital signal processing; DAC: Digital-to-analogue converter; OOB: Out of band.

Authors' contributions

RZ designed the envelope conversion algorithm and the test circuitry, YS helped with the simulation and experiment, and YW proposed the initial idea of this research and helped with manuscript writing. All authors read and approved the final manuscript.

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Availability of data and materials

The datasets used and/or analysis during the current study are available from the corresponding author on reasonable request.

Declarations

Competing interests

The authors declare that they have no competing interests.

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